Jawaharlal College of Engineering and Technology
Jawahar Gardens,Mangalam,Palakkad,Kerala
AICTE Approved,Affiliated APJAKTU,ISO 9001:2015 Certified

ECT202
ANALOG CIRCUITS
(2019 Scheme)

LECTURE NOTES

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INSTITUTION VISION

- Emerge as a centre of excellence for professional education to produce high quality engineers and entrepreneurs for the development of the region and the Nation.

INSTITUTION MISSION

- To become an ultimate destination for acquiring latest and advanced knowledge in the multidisciplinary domains.
- To provide high quality education in engineering and technology through innovative teaching-learning practices, research and consultancy, embedded with professional ethics.
- To promote intellectual curiosity and thirst for acquiring knowledge through outcome based education.
- To have partnership with industry and reputed institutions to enhance the employability skills of the students and pedagogical pursuits.
- To leverage technologies to solve the real life societal problems through community services.

DEPARTMENT VISION

To become a centre of academic excellence in the field of ECE in order to raise engineer with international standards with ethical values & ability to apply acquired knowledge for solving technologically challenging societal problems.

DEPARTMENT MISSION

- To impart high quality education through innovative and comprehensive instructional materials in the area of ECE.
- To develop research linkages with organizations in India & abroad and to establish industry interface to expose students to the industrial environment.
- To develop a committed group of faculty striving for excellence in teaching & research in the emerging fields in ECE.
- To provide ethical & value based education for promoting essence of responsibility towards nation building social causes and environmental conservation.

PEOs OF THE DEPARTMENT

- To Provide a Solid Foundation in Electronics and Communication Engineering Essentials with an Attitude to Pursue Higher Education, Participation in Research & Development Activities, and Involvement in Lifelong Learning & Professional Development.
- Obtain In-Depth Knowledge of the Core Discipline of Electronics & Communication Engineering so that they will be able to Establish Engineering Standards and Overcome Realistic Constraints in Systematic Engineering Processes with the Incorporation of Industries' Expectations and Design Socially Accepted and Economically Feasible Solutions in the Respective Fields.
- To Make the Student Communicate Effectively, Lead a Team with Good Leadership Traits, and Exhibit Professional Conduct.

PSOs OF THE DEPARTMENT

The students will be able to

- Apply Science & Mathematics through Differential and Integral Calculus; To Solve Complex Electronics and Communication Engineering Problems.
- Attain the Ability to Interpret the Basic Concepts and Methods of Electronic Systems and Technical Specifications to Provide Accurate Solutions.
- Utilize Electronic Current Advances (Both Software and Hardware) for the Design and Analysis of Complex Electronic Frameworks in Research Activities.

ECT202	ANALOG CIRCUITS	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to develop the skill of analyse and design of different types of analog circuits using discrete electronic components.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO 1	Design analog signal processing circuits using diodes and first order RC circuit
CO 2	Analyse basic amplifiers using BJT and MOSFET
CO 3	Apply the principle of oscillator and regulated power supply circuits.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										2
CO 2	3	3										2
CO 3	3	3										2

Assessment Pattern

Bloom's Category		Continuous Assessment Tests		End Semester Examination
		1	2	
Remember	K1	10	10	10
Understand	K2	20	20	20
Apply	K3	20	20	70
Analyse	K4			
Evaluate				
Create				

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Course Level Assessment Questions

Course Outcome 1 (CO1): Design analog signal processing circuits using diodes and first order RC circuit.

1. For the given specification design a differentiator / integrator circuit.
2. For the given transfer characteristics design clipping / clamping circuit.
3. Design first order RC low-pass / high-pass circuit for the given specification.

Course Outcome 2 (CO2): Analyse basic amplifiers using BJT.

1. For the given transistor biasing circuit, determine the resistor values, biasing currents and voltages.
2. Design a RC coupled amplifier for a given gain.
3. Analyse the frequency response of BJT RC coupled amplifier using hybrid π model.

Course Outcome 2 (CO2): Analyse basic amplifiers using MOSFET.

1. Perform DC analysis of MOSFET circuits.
2. Design a common source amplifier.
3. Deduce the expression for voltage gain of CS stage with diode-connected load.

Course Outcome 2 (CO2): Analyse basic feedback amplifiers using BJT and MOSFET

1. Deduce the expression for voltage gain, input impedance and output impedance of the four feedback amplifier topologies.
2. Design practical discrete amplifiers for the four feedback amplifier topologies.

Course Outcome 3 (CO3): Apply the principle of oscillator and regulated power supply.

1. Design oscillator using BJT to generate sine wave for the given frequency.
2. Deduce the expression for maximum efficiency of class B power amplifiers.
3. Illustrate the DC and AC load line in transformer coupled class A power amplifiers.
4. Design voltage regulator for the given specifications.

SYLLABUS

Module 1:

Wave shaping circuits: First order RC differentiating and integrating circuits, First order RC low pass and high pass filters.

Diode Clipping circuits - Positive, negative and biased clipper. Diode Clamping circuits - Positive, negative and biased clamper.

Transistor biasing: Need, operating point, concept of DC load line, fixed bias, self bias, voltage divider bias, bias stabilization.

Module 2:

BJT Amplifiers: RC coupled amplifier (CE configuration) – need of various components and design, Concept of AC load lines, voltage gain and frequency response.

Small signal analysis of CE configuration using small signal hybrid-pi model for mid frequency and low frequency. (gain, input and output impedance).

High frequency equivalent circuits of BJT, Miller effect, Analysis of high frequency response of CE amplifier.

Module 3:

MOSFET amplifiers: MOSFET circuits at DC, MOSFET as an amplifier, Biasing of discrete MOSFET amplifier, small signal equivalent circuit. Small signal voltage and current gain, input and output impedance of CS configuration. CS stage with current source load, CS stage with diode-connected load.

Multistage amplifiers - effect of cascading on gain and bandwidth. Cascode amplifier.

Module 4 :

Feedback amplifiers: Effect of positive and negative feedback on gain, frequency response and distortion. The four basic feedback topologies, Analysis of discrete BJT circuits in voltage-series and voltage-shunt feedback topologies - voltage gain, input and output impedance.

Oscillators: Classification, criterion for oscillation, Wien bridge oscillator, Hartley and Crystal oscillator. (working principle and design equations of the circuits; analysis of Wien bridge oscillator only required).

Module 5:

Power amplifiers: Classification, Transformer coupled class A power amplifier, push pull class B and class AB power amplifiers, complementary-symmetry class B and Class AB power amplifiers, efficiency and distortion (no analysis required)

Regulated power supplies: Shunt voltage regulator, series voltage regulator, Short circuit protection and fold back protection, Output current boosting.

Text Books

1. Robert Boylestad and L Nashelsky, “Electronic Devices and Circuit Theory”, 11/e Pearson, 2015.
2. Sedra A. S. and K. C. Smith, “Microelectronic Circuits”, 6/e, Oxford University Press, 2013.

Reference Books

1. Razavi B., “Fundamentals of Microelectronics”, Wiley, 2015
2. Neamen D., “Electronic Circuits, Analysis and Design”, 3/e, TMH, 2007.
3. David A Bell, “Electronic Devices and Circuits”, Oxford University Press, 2008.
4. Rashid M. H., “Microelectronic Circuits - Analysis and Design”, Cengage Learning, 2/e,2011
5. Millman J. and C. Halkias, “Integrated Electronics”, 2/e, McGraw-Hill, 2010.

Course Contents and Lecture Schedule

No	Topic	No. of lectures
1	**Wave shaping circuits**	
1.1	Analysis and design of RC differentiating and integrating circuits	2
1.2	Analysis and design of First order RC low pass and high pass filters	2
1.3	Clipping circuits - Positive, negative and biased clipper	1
1.4	Clamping circuits - Positive, negative and biased clamper	1
	Transistor biasing	
1.5	Need of biasing, operating point, bias stabilization, concept of load line	1
	Design of fixed bias, self bias, voltage divider bias.	2
2	**BJT Amplifiers**	
2.1	Classification of amplifiers, RC coupled amplifier (CE configuration) – need of various components and design, Concept of AC load lines.	2
2.2	Small signal analysis of CE configuration using small signal hybrid π model for mid frequency. (gain, input and output impedance).	3
2.3	High frequency equivalent circuits of BJT, Miller effect, Analysis of high frequency response of CE amplifier. voltage gain and frequency response	4
3	**MOSFET amplifiers**	
3.1	MOSFET circuits at DC, MOSFET as an amplifier, Biasing of discrete MOSFET amplifier,	2
3.2	Small signal equivalent circuit. Small signal voltage and current gain, input and output impedances of CS configuration.	3

3.3	CS stage with current source load, CS stage with diode-connected load.	2
3.4	**Multistage amplifiers** - effect of cascading on gain and bandwidth. Cascode amplifier.	2
4	**Feedback amplifiers**	
4.1	Properties of positive and negative feedback on gain, frequency response and distortion.	1
4.2	Analysis of the four basic feedback topologies	2
4.3	Analysis of discrete circuits in each feedback topologies -voltage gain, input and output impedance	3
	Oscillators	
4.4	Classification, criterion for oscillation	1
	Wien bridge oscillator, Hartley and Crystal oscillator. (working principle and design equations of the circuits; analysis not required).	2
5	**Power amplifiers**	
5.1	Classification, Transformer coupled class A power amplifier	1
5.2	push pull class B and class AB power amplifiers, complementary-symmetry class B and Class AB power amplifiers, efficiency and distortion (no analysis required)	3
	Linear Regulated power supplies	
5.3	Principle of Linear Regulated power supplies, Shunt voltage regulator	1
5.4	Series voltage regulator, Short circuit protection and fold back protection, Output current boosting	2

Assignment:

Atleast one assignment should be simulation of different types of transistor amplifiers on any circuit simulation software.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, (**Model Question Paper)**

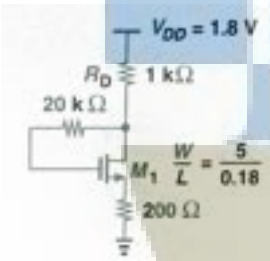
Course Code: ECT202

Course Name: ANALOG CIRCUITS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer ALL Questions. Each Carries 3 mark.

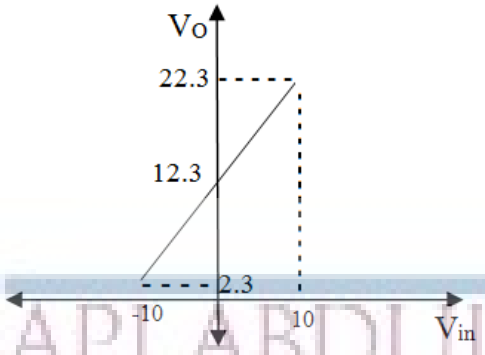
1	Design the first order RC high pass filter with cut off frequency 2Kz.	3	K3
2	Describe about the double ended clipping.	3	K2
3	Differentiate between DC and AC load lines.	3	K2
4	What is the significance of Miller effect on high frequency amplifiers?	3	K1
5	What are the effects of cascading in gain and bandwidth of an amplifier?	3	K1
6	Calculate the drain current if $\mu_n C_{ox}$ = 100 μA/V^2, V_{TH} = 0.5V and λ = 0 in the following circuit. 	3	K3
7	Illustrate the effect of negative feedback on bandwidth and gain of the amplifier.	3	K2
8	Explain the criteria for an oscillator to oscillate.	3	K1
9	How to eliminate cross over distortion in class-B power amplifier?	3	K2
10	What is line regulation and load regulation in the context of a voltage regulator?	3	K2

PART – B

Answer one question from each module; each question carries 14 marks.

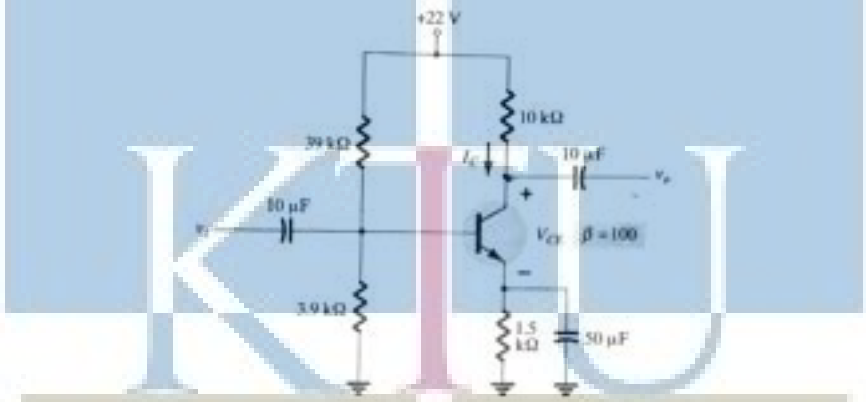
Module - I

11 a	Design a differentiator circuit for a square wave signal with Vpp=10 and frequency 10KHz.	6	CO1 K3
b.	Design a clamper circuit to get the following transfer characteristics, assuming voltage drop across the diodes 0.7V.	8	CO1 K3



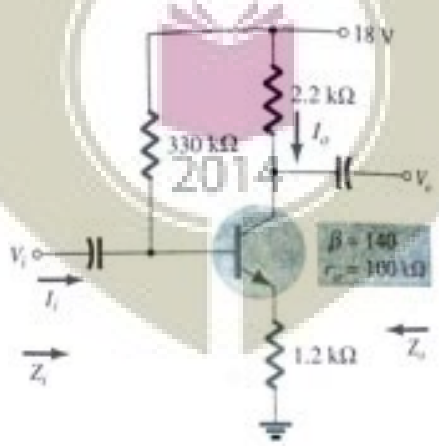
OR

12 a	Explain the working of an RC differentiator circuit for a square wave input with period T. Sketch its output waveform for RC ≫ T, RC ≪ T and RC = T.	5	K2 CO1
b.	With reference to the following circuit, draw the load line and mark the Q point of the Silicon BJT transistor.	9	K3 CO2



Module - II

13	For the following RC coupled amplifier determine r_e , Z_i, Z_o and A_v .	14	K3 CO2



OR

14	a	Draw the high frequency hybrid π model of BJT in CE configuration and explain the significance of each parameter.	6	K2 CO2
	b	Analyse BJT RC coupled amplifier in CE configuration at high frequency using hybrid π model.	8	K2 CO2

Module - III

15	a	Draw the circuit of a common source amplifier using MOSFET. Derive the expressions for voltage gain and input resistance from small signal equivalent circuit.	7	K2 CO2
	b.	How wide bandwidth is obtained in Cascode amplifier ?	7	K2 CO2

OR

16		Draw the CS stage with current source load and deduce the expression for voltage gain of the amplifier	14	K3 CO2

Module - IV

17		Give the block schematic of current-series feedback amplifier configuration and deduce the expression for gain, input impedance and output impedance with feedback. Design a practical circuit for this current-series feedback amplifier.	14	K3 CO2

OR

18	a	Design wein-bridge oscillator using BJT to generate 1KHz sine wave.	8	K3 CO3
	b	Explain the working principle of crystal oscillator	6	K2 CO3

Module - V

19		Illustrate the working principle of complementary-symmetry class B power amplifiers and deduce the maximum efficiency of the circuit	14	K2 CO2

OR

20		Design a discrete series voltage regulator with short circuit protection for regulated output voltage 10V and maximum current 100mA.	14	K3 CO3

Simulation Assignments (ECT202)

The following simulations can be done in QUCS, KiCad or PSPICE.

1. Design and simulate a voltage series feedback amplifier based on BJT/ MOSFET. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquits plot and understand its stability
2. Design and simulate a voltage shunt feedback amplifier based on BJT/ MOSFET. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquits plot and understand its stability
3. Design and simulate series voltage regulator for output voltage $V_O = 10V$ and output current $I_O = 100mA$ with and without short circuit protection and to test the line and load regulations.
4. Design and simulate Wien bridge oscillator for a frequency of $5\,kHz$. Run a transient simulation and observe the output waveform.
5. Design and simulate Colpitts oscillator for a frequency of $455\,kHz$. Run a transient simulation and observe the output waveform.
6. Design and simulate a current series feedback amplifier based on BJT. Observe the input and output signals. Plot the AC frequency response. Observe the Nyquits plot and understand its stability
7. Design and simulate Hartley oscillator for a frequency of $455\,kHz$. Run a transient simulation and observe the output waveform.
8. Design and simulate clipping circuits that clips the $10\,V$ input sinusoid
   - at $+3.5\,V$ and at $-4.2\,V$
   - at $+2.5\,V$ and at $+4.2\,V$
   - at $-2.5\,V$ and at $-4.2\,V$

   with Si diodes

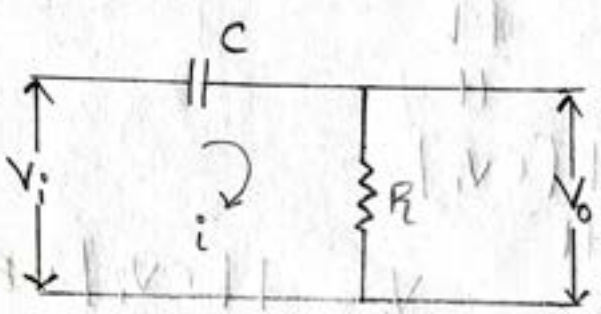
10/2/23

MODULE I
WAVE SHAPING CIRCUITS

RC Differentiator:

A circuit in which output is directly proportional to the derivative of input is known as a Differentiating circuit or Differentiator.

$$O/P \propto \frac{d(i/p)}{dt}$$



A differentiating circuit is a single RC network when the O/p is taken across the resistor. If a DC or a constant i/p is given as the input then O/p will be equal to zero.

In order to achieve good differentiation the following 2 conditions are to be satisfied

1. The time constant RC of the input should be much smaller than the time period of i/p signal.
2. The value of X_C should be 10 or more times greater than R at operating frequency.

let V_i be the i/p voltage and V_o be the o/p voltage.

Now the charge q in the capacitor is;

$$q = CV_c$$

$\therefore$ the capacitive reactance is much greater than R,

$$V_c \simeq V_i$$

$$\rightarrow q = CV_i$$

Then the current through the capacitor is given by, $i = \frac{dq}{dt}$

$$i = \frac{d[CV_i]}{dt}$$

$$\therefore V_o = iR \qquad V_o = \frac{d[CV_i]}{dt} \times R$$

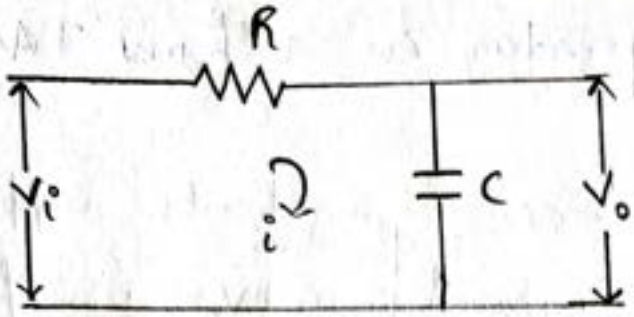
$$V_o = RC \frac{dV_i}{dt}$$

$$\therefore \boxed{V_o \propto \frac{dV_i}{dt}}$$

RC Integrator:

It is a circuit whose o/p voltage is directly proportional to the integral of i/p voltage.

ie; $V_o \propto \int V_i$



Inorder to achieve good integration

1. The time constant RC should be very large compared to time period of i/p variable. $RC > 16T$
2. The value of R should be 10 or more time the capacitive reactance X_C.

$$V_R \simeq V_i \quad \because R >> X_C$$

$$\therefore i = \frac{V_R}{R} = \frac{V_i}{R}$$

$$q = \int i\,dt$$

$$q = \int \frac{V_i}{R}\,dt$$

$$V_o = \frac{1}{C}\int \frac{V_i}{R}\,dt$$

$$V_o = \frac{1}{RC}\int V_i\,dt$$

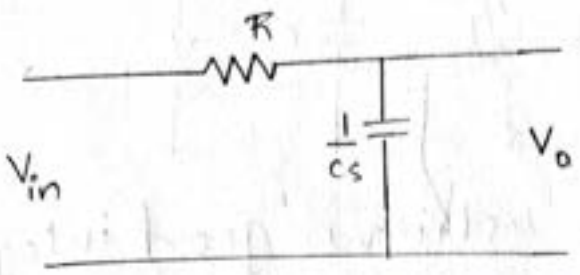
$$\boxed{V_o \propto \int V_i}$$

$$V_o = \frac{q}{C}.$$

$$q = CV.$$

27/2/23

RC Integrator as a low Pass Filter [LPF]



$A_v \Rightarrow V_{ge}$ gain

$S = j\omega$

$= j2\pi f$

$f_H = \frac{1}{2\pi RC}$

cutoff frequency

$f = f_H = \frac{1}{\sqrt{2}} A_v$

Here, the voltage gain A_v;

$$A_v = \frac{V_{out}}{V_{in}}$$

from figure we can find V_{out}

$$= V_{out} = V_{in} \times \frac{1/cs}{R + 1/cs} \quad (V_{ge} \text{ Voltage Divider Rule})$$

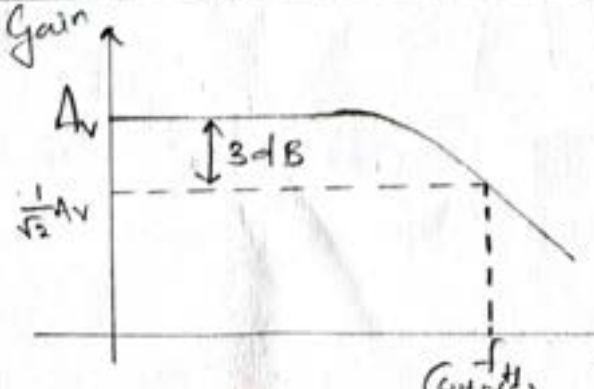
$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{Rcs + 1} = \frac{1}{RCj2\pi f + 1}$$

$$A_v = \frac{1}{1 + j(f/f_H)}$$

$f_H = \frac{1}{2\pi RC}$

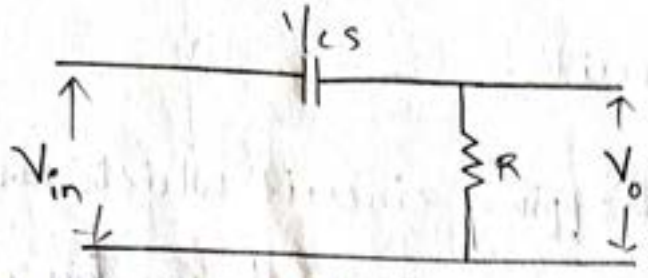
Magnitude, $|A_v| = \frac{1}{\sqrt{1 + (f/f_H)^2}}$

low Pass characteristics:



LPF response when $f = f_H, \frac{1}{\sqrt{2}} A_v$

RC Differential HPF



Here the voltage gain, $A_v = \frac{V_{out}}{V_{in}}$

from figure,

$V_{out} = V_{in} \times \frac{R}{\frac{1}{Cs} + R}$ [Voltage division rule] $\frac{1+R}{Cs}$

$\frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{1}{RCs}}$ $s = j\omega = j2\pi f$

$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{1}{RCj2\pi f}}$ $\frac{1}{2\pi RC} = f_L$ cut off

$= \frac{1}{1 + \frac{f_L}{f}} = \frac{1}{1 + \frac{1}{j}\left(\frac{f_L}{f}\right)}$ $\frac{1}{j} = -j$

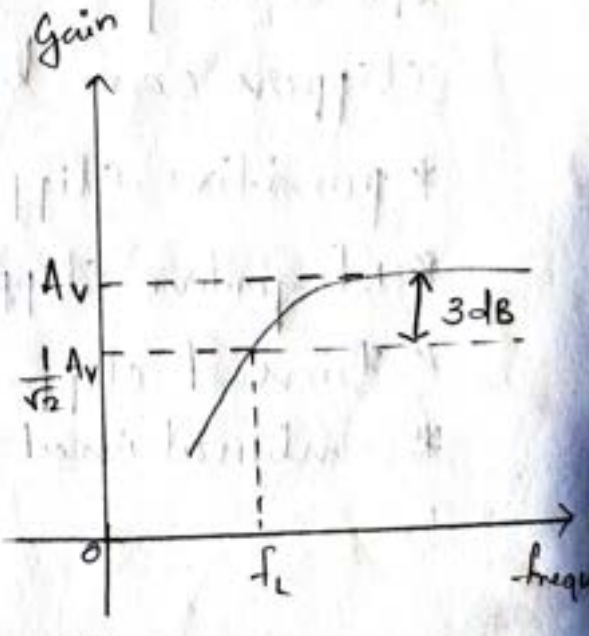
$A_v = \frac{1}{1 - j\left(\frac{f_L}{f}\right)}$

$|A_v| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$

High Pass characteristics ⇒

HPF response.

When $f_o = f_L$, $A_v = \frac{1}{\sqrt{2}}$ $\therefore V_{out} = \frac{1}{\sqrt{2}} V_m$



Wave Shaping Circuits.

1. Clipping Circuits:

A wave shapping circuit which controls the shape of output waveform by removing a portion of applied wave is known as clipping circuits.

Half wave rectifier is an example of clipper.

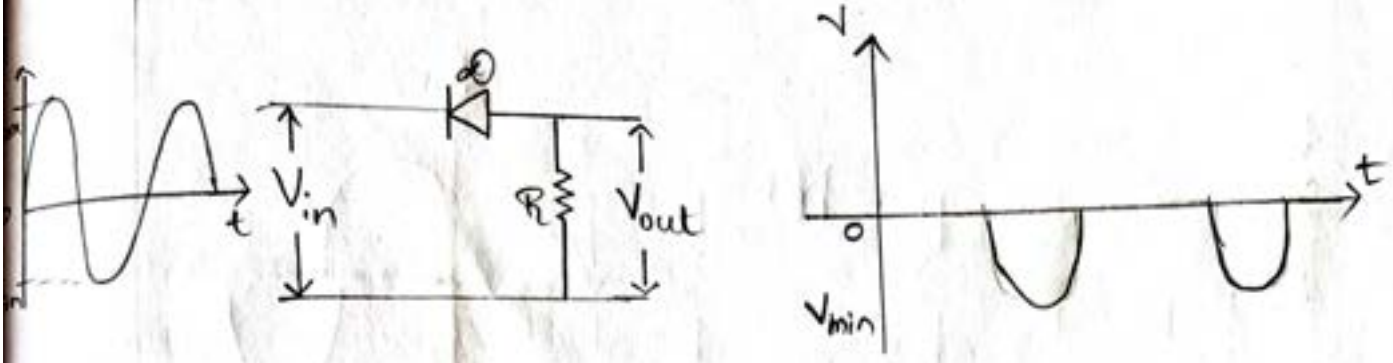
According to the configuration used the clipper can be

* Series diode clipper
* Shunt / parallel diode clipper
* Combination of diode, resistance and power supply.

According to the level of clipping, the clippers can be

* positive clipper
* Negative clipper
* Biased clipper
* Combinational clipper.

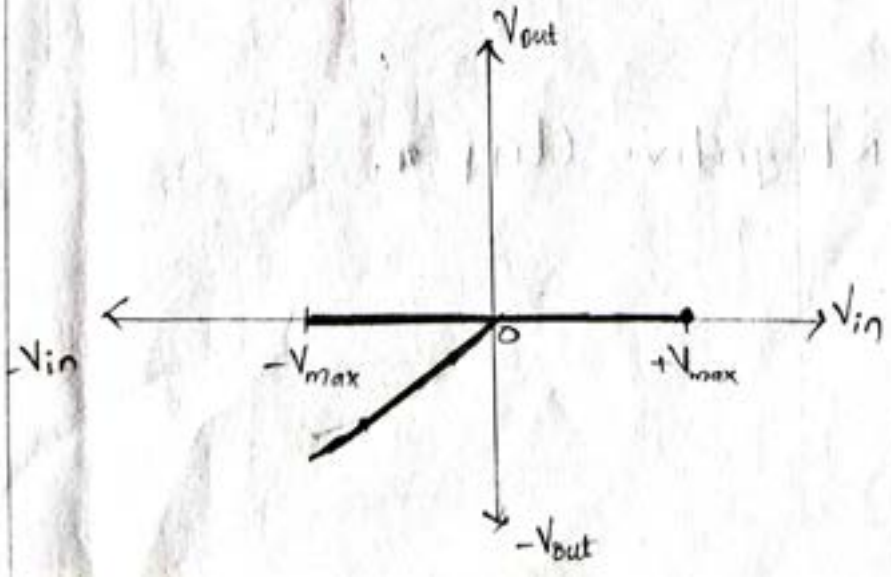
1. Positive Clipper:



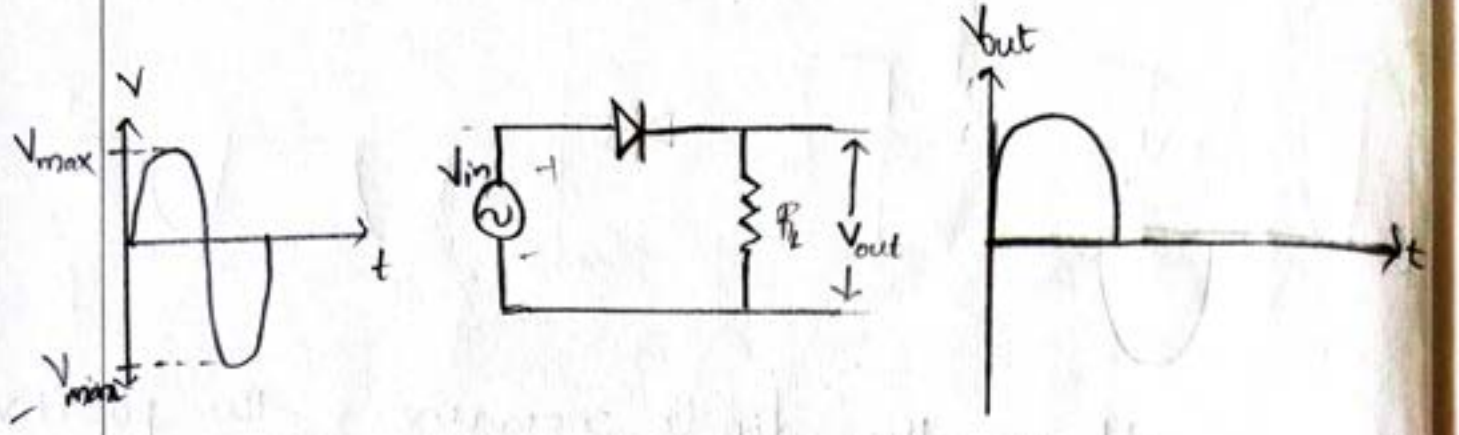
Here, the diode removes the positive half cycle. So it is known as positive clipper. During the +ve half cycle of i/p, the diode becomes reverse biased and so the current will not flow through the resistor. So the o/p voltage is zero.

During the -ve half cycle, the diode becomes forward biased and the current flows through the resistor and entire -ve half cycle appears across the resistor.

Transfer characteristics:



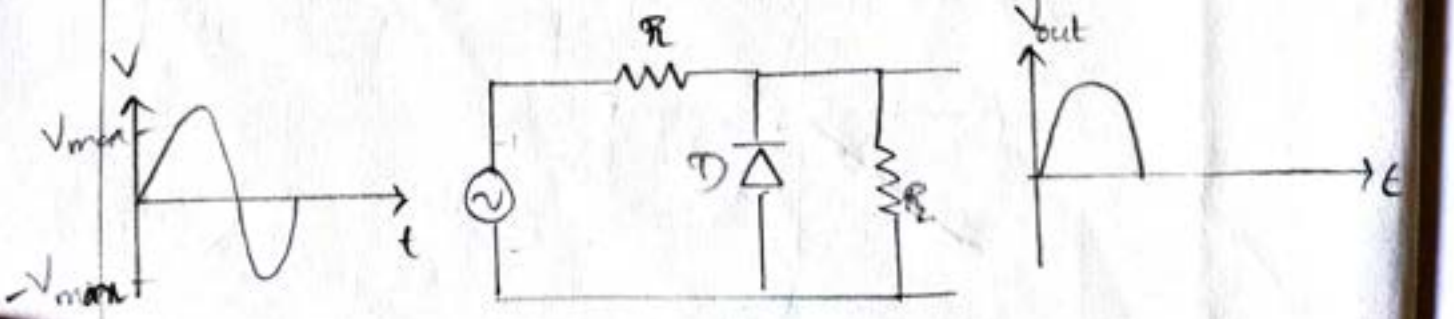
1/3/23 Negative Clipper. (Basics)



Negative clipper removes -ve half cycle of i/p signal from o/p. Here, during +ve half cycle of input diode becomes forward biased and thus act as short circuit. The entire i/p (+ve half cycle) appears across the load [R_L].

When negative half cycle arrives, it makes the diode reverse biased and it act as an open circuit. Thus the o/p current and o/p voltage becomes two.

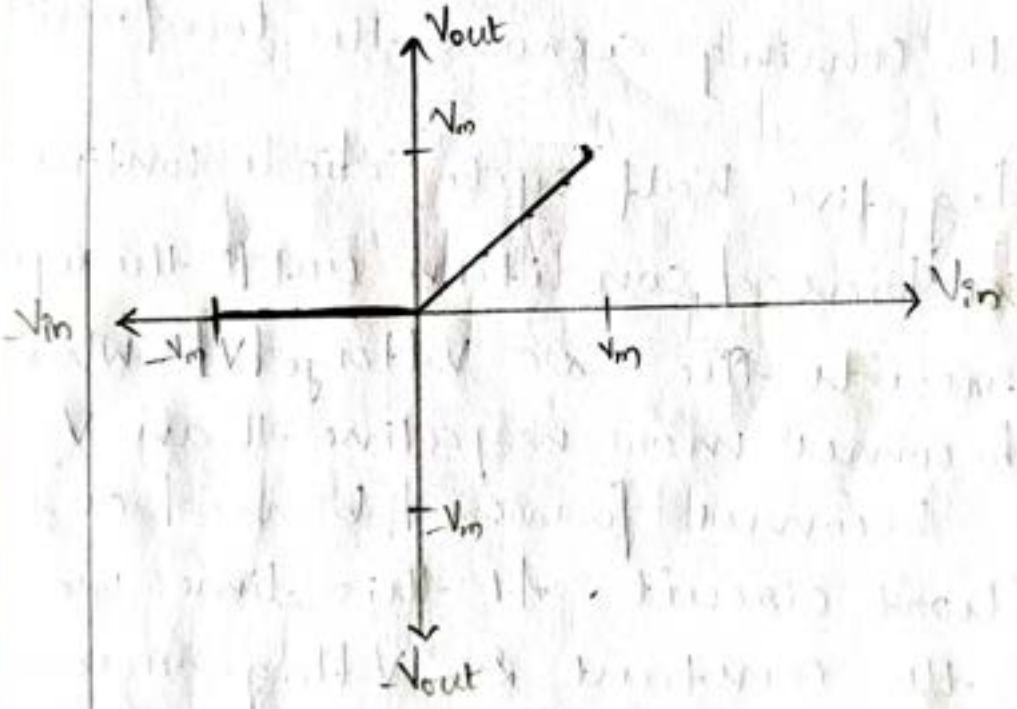
Shunt Negative Clipper.



In Shunt negative clipper, during +ve half cycle of i/p, diode becomes reverse biased and act as open circuit. The entire current will flow through load resistance and we will get +ve half cycle of i/p as output.

During -ve half cycle, diode becomes forward biased and act as Short circuit, So the o/p becomes zero.

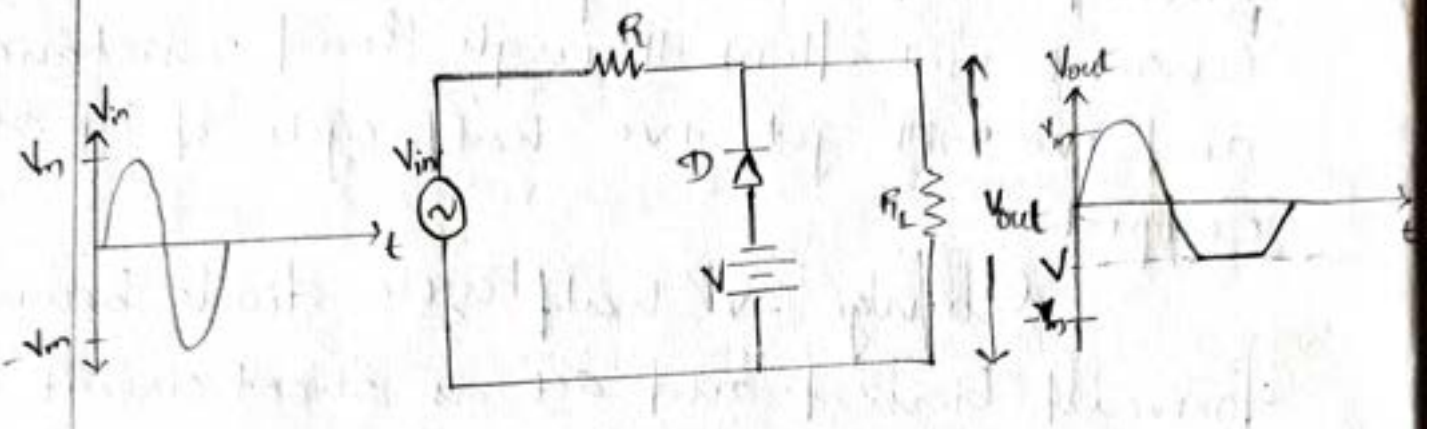
Transfer Characteristics:



Biased clipper.

In order to remove a small portion of positive or negative half cycle of input voltage, biased clippers are used.

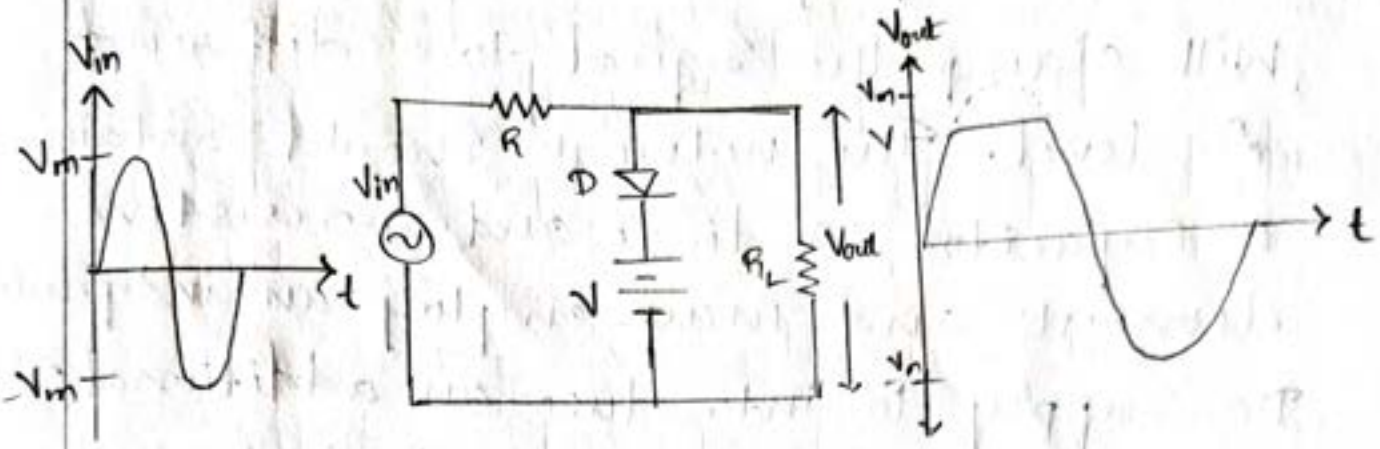
*Biased Negative Clipper:



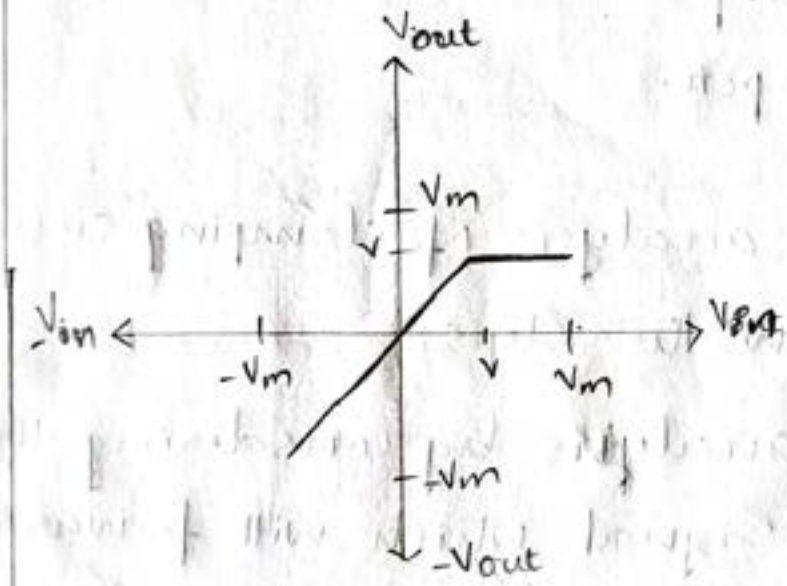
Here, during +ve half cycle of i/p diode becomes reversed and so the entire +ve half cycle coming across the load resistance [R_L].

Negative half cycle, diode continues in reverse biased condition untill the input signal exceeds the DC voltage [V]. When the i/p becomes more negative than V, the diode becomes forward biased and act as short circuit. At this time we will get the constant DC voltage across R_L. When the input swings back again the diode becomes reversed and output follows the input:

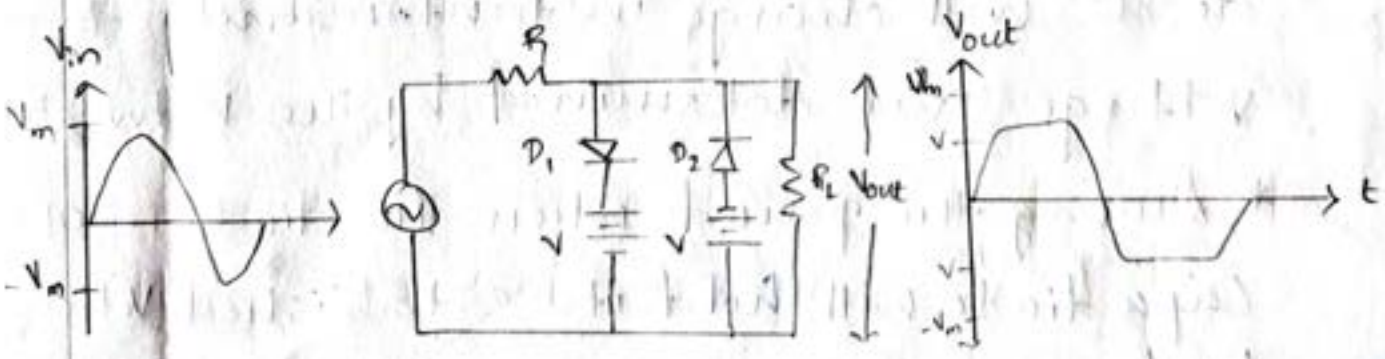
* Biased positive clipper.



Transfer characteristic.



Combinational clipper.



2/8/23

Clamper Circuits.

The clamping network is the one that will clamp the signal to a different Dc level. The network should contain a capacitor, a diode and a resistive element and may employ an independent Dc supply to introduce an additional shift. The clamping circuits can be:

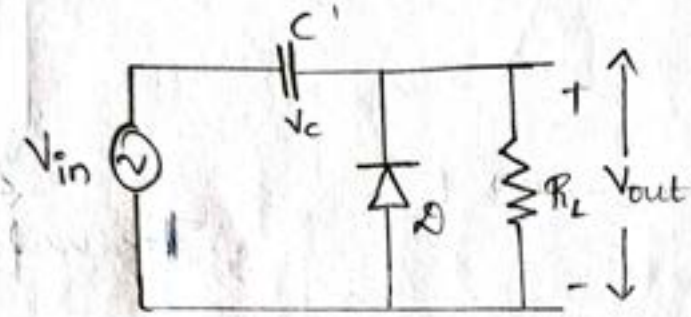
* Positive clamper
* Negative clamper
* Biased clamper.

For the analysis of clamping circuit, we can follow the steps:

* Start the analysis by considering that part of i/p signal which will forward bias the diode.
* During the period that the diode is ON, diode will charge instantaneously to a voltage level determined by the network.
* During the period when the diode is OFF, Capacitor diode will hold its established voltage level.

* keeping in mind the General rule that the total voltage swing of o/p must match the voltage swing of i/p signal.

Positive clamper.



During negative half cycle of input diode becomes forward and so the capacitor charges to the maximum available voltage. By applying KVL,

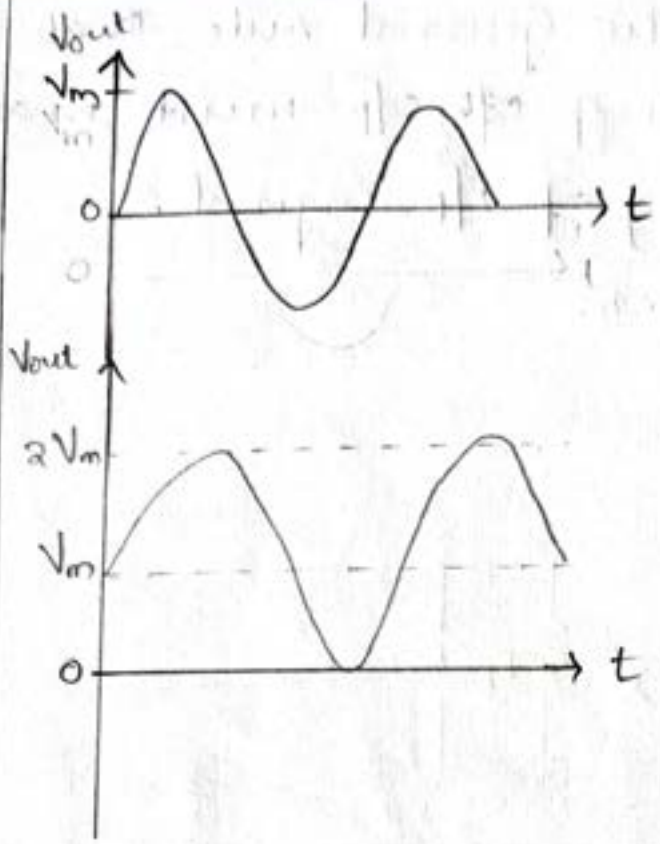
$$-V_{in} + V_c = 0$$

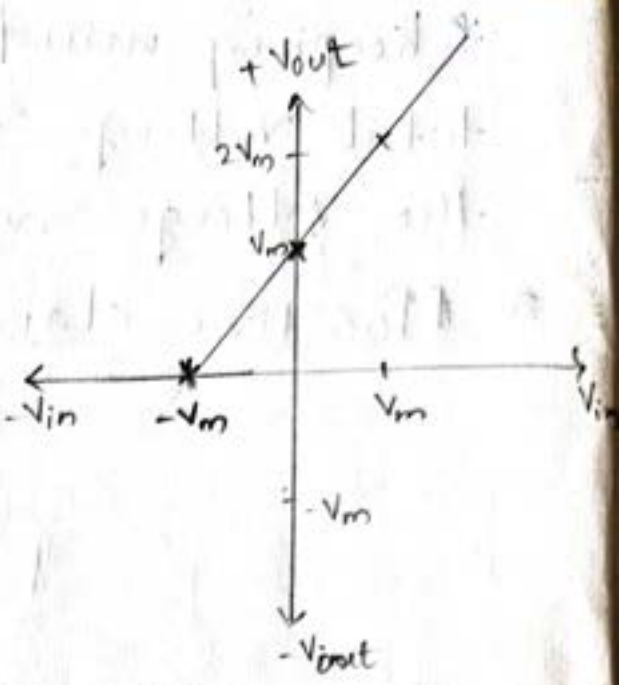
$$V_c = V_m.$$

During the +ve half cycle, diode becomes reverse biased. By applying KVL,

$$V_m + (V_m) - V_{out} = 0$$

$$V_{out} = 2V_m.$$

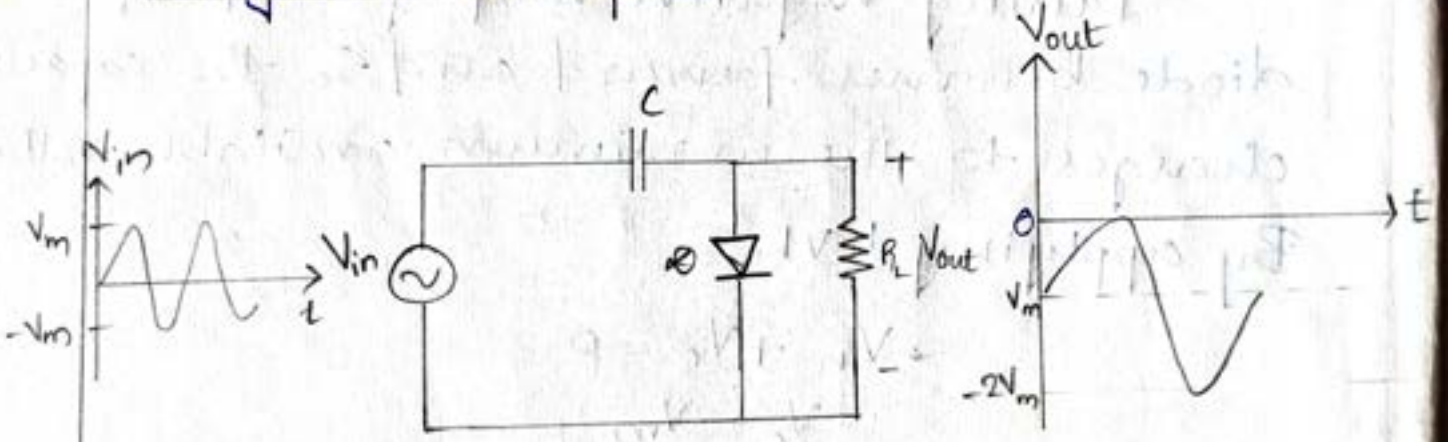


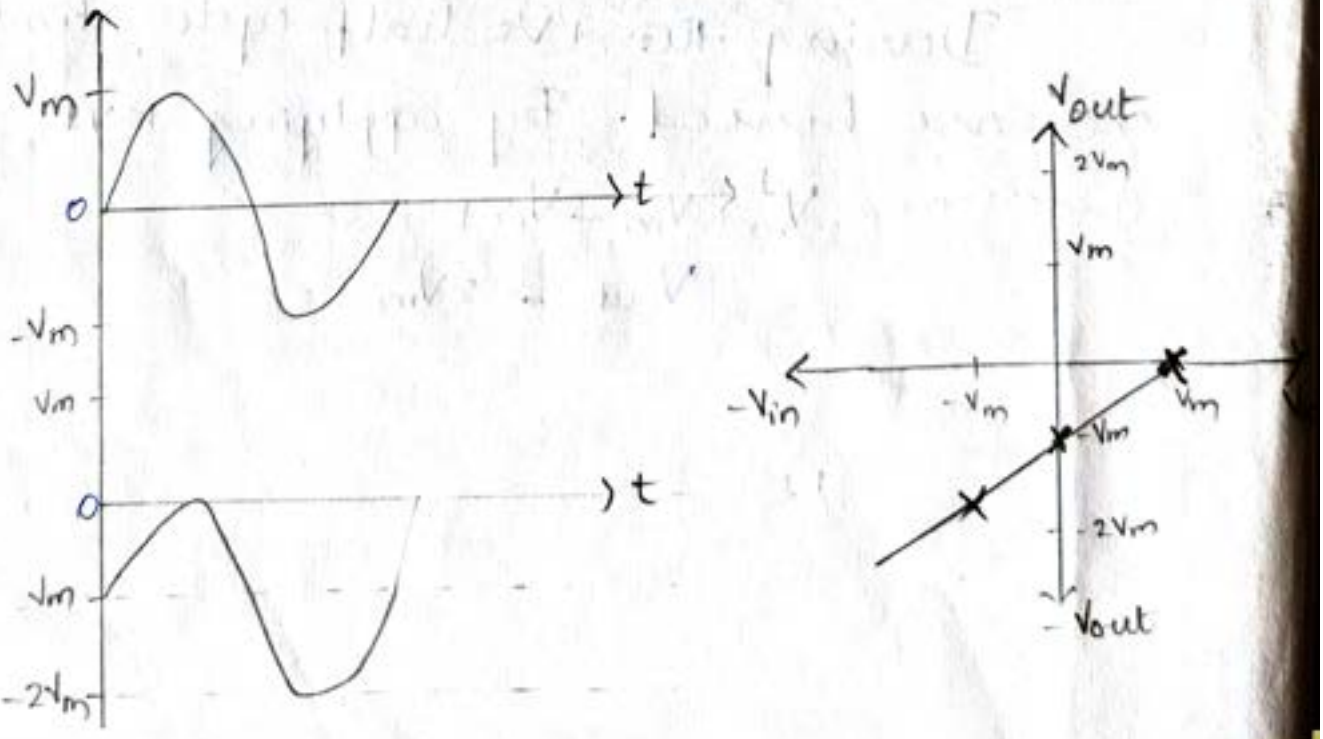


Transfer chara.

3/3/23

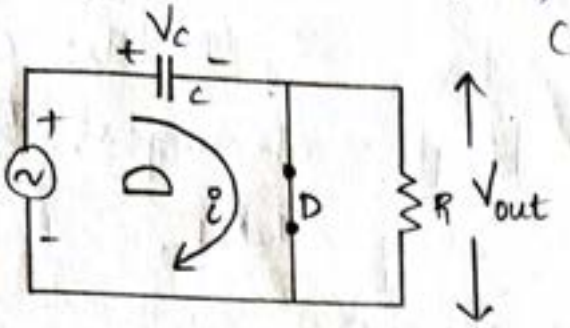
Negative clamper:





During +ve half cycle, the capacitor charges towards the maximum i/p voltage. By applying KVL,

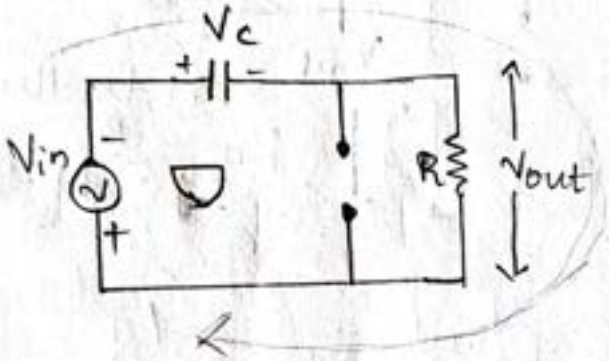
(FB)



$$V_{in} - V_c = 0$$

$$V_c = V_{in} = V_m.$$

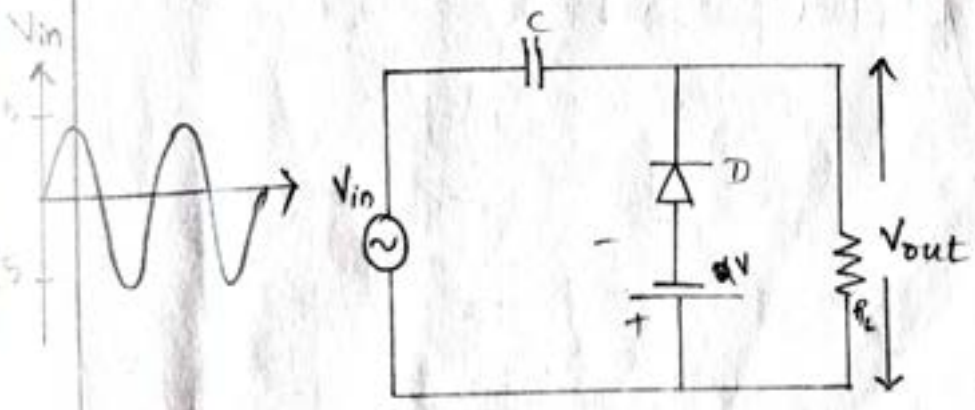
During -ve half cycle, the capacitor holds the charge and the o/p can be find out by applying KVL,

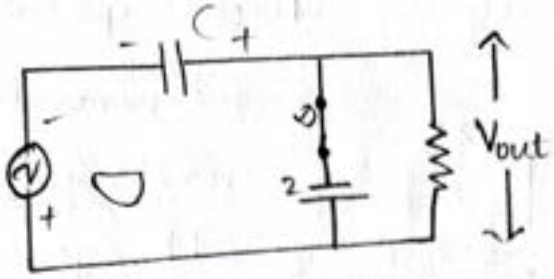


$$-V_{in} - V_c - V_{out} = 0$$

$$V_{out} = -2V_m. \quad [\because V_{in} = V_c = V_m]$$

Biased positive clamper.

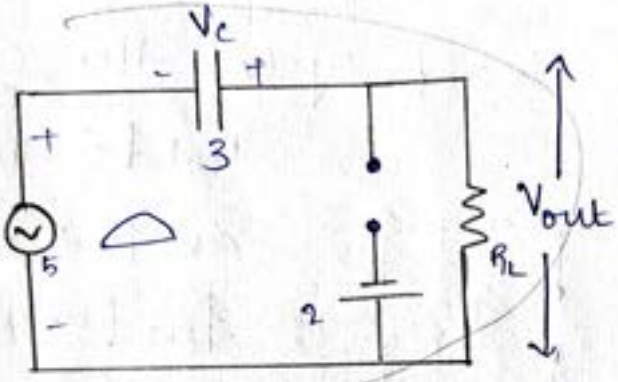




During negative half cycle, the capcitor charges. By applying KVL,

$$-5 + V_c + 2 = 0$$

$$V_c = 3.$$



During +ve half cycle, the capacitor holds the charge. By applying KVL,

$$5 + 3 - V_{out} = 0$$

$$5 + 3 = V_{out}$$

$$V_{out} = 8V.$$

General Expression

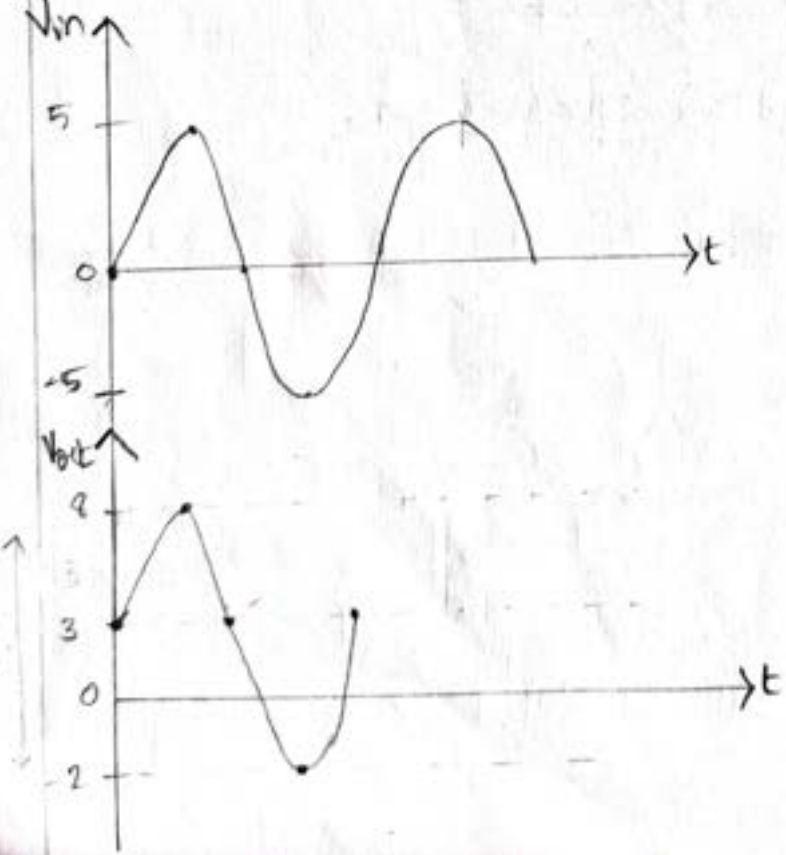
$$V_{out} = V_{in} + V_c$$

$V_{out} = 0 + 3 = 3$

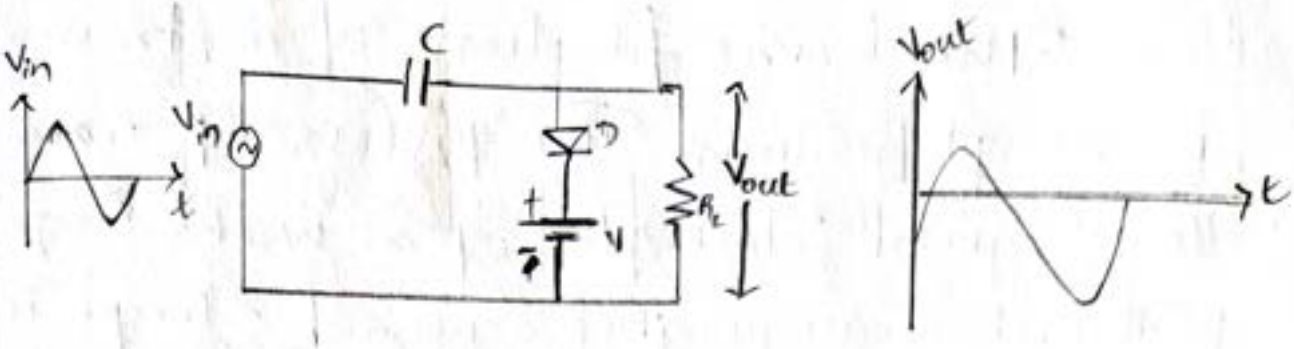
$V_{out} = 5 + 3 = 8$

$= -5 + 3 = -2$

$= 0 + 3 = 3$



Biased Negative clamper:



7/3/23

Transistor Biasing.

The basic function of a transistor is amplification. The process of raising the signal strength of a week signal without changing its general shape is known as faithful amplification. For faithful amplification it is necessary that

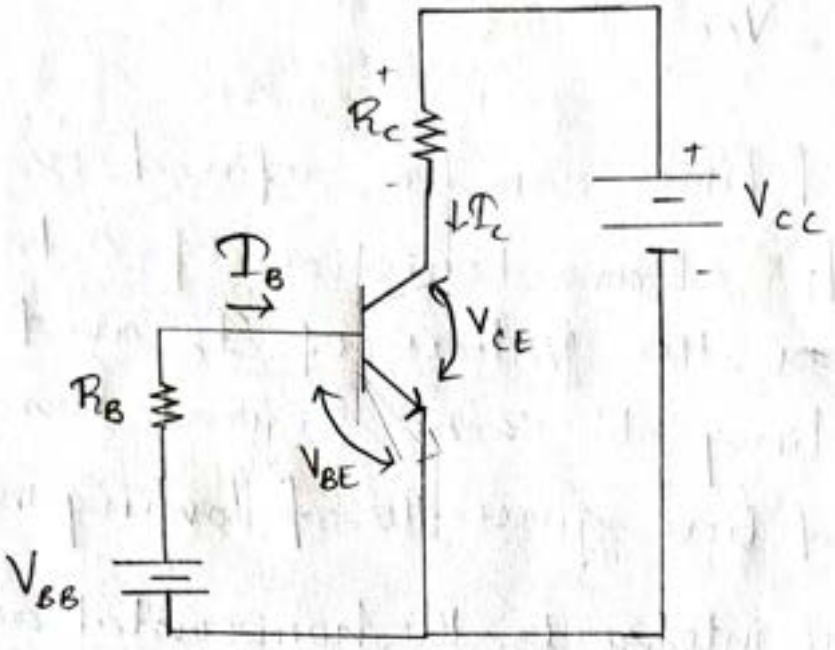
1. The emitter-base junction forward biased.
2. Collector-base junction reverse biased.
3. Proper maintenance of zero signal voltage and current.

The proper flow of zero signal collector current I_c and the voltage V_{CE} during the passage of signal is called transistor biasing.

Operating point and DC load line.

For the operation of transistor, whether the signal is present or not a fixed level of voltage and current is needed. These value of voltage and current define a point at which the transistor operates. This point is known as Operating point.

Quiscent point or Q point.



By applying KVL, in the o/p side

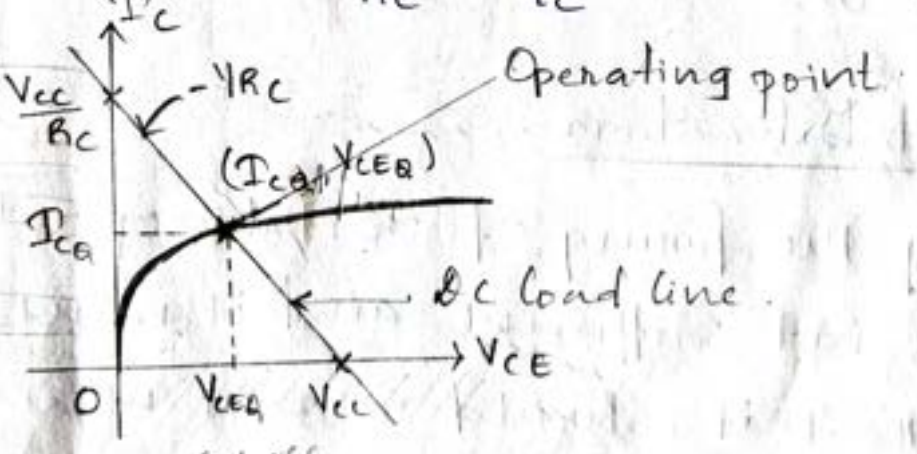
$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} \quad \text{——} (1)$$

$y = mx + c$

$I_C = \frac{-1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$



Equation (1) is analogous to the equation of a line ($y = mx + c$). In equation (1), for $V_{CE} = 0$;

$$I_C = \frac{V_{CC}}{R_C}$$

When, $I_C = 0$

$$V_{CE} = V_{CC}$$

Dc load line can be defined as a line on the o/p characteristics of a transistor which gives the values of I_C and V_{CE} corresponding to zero signal condition.

Dc load line gives the following informations:

1. load line intersects the horizontal axis at a point marked V_{CC} which is called transistor cut off point where $I_C = I_B = 0$
2. The load line intersects on Vertical Y axis at a point marked as V_{CC}/R_C, $I_C = \frac{V_{CC}}{R_C}$ which is called Saturation point where $V_{CE} = 0$.

8/3/23

Bias Stabilization.

Only the fixing of suitable operating point is not sufficient and it must also ensure that it should remain where it was fixed. There are two reasons for operating point to shift:

1. Transistor parameters are temperature

dependent

2. The parameters such as β changes from unit to unit.

The maintainance of operating point stable (independent of temp Variation and Variation of transistor parameters) is known as bias stabilization.

Thermal run away.

The flow of current in collector circuit produces heat at collector circuit. This increases the temperature and produces more minority carriers in the base-collector junction. Since more bonds are broken resulting leakage current I_{CO} [I_{CBO}] to increase.

$$I_C = \beta I_B + (\beta+1) I_{CBO}$$
$$= \beta I_B + I_{CEO}$$

, $I_{CEO} = (\beta+1) I_{CBO}$

The increase in I_{CBO} intern increases I_{CEO} which increases the collector current I_C. The raise in I_C increases the heat generated and finally burns the transistor. This is known as thermal run away.

Stability factor:

Stability factor S is defined as the rate of change of collector current w.r.t I_{C_0} keeping β and V_{BE} as constants.

$$S = \frac{\partial I_C}{\partial I_{C_0}} \Big| \beta, V_{BE} \text{ constant}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \Big| \beta \& I_{C_0} \text{ constant}$$

$$S'' = \frac{\partial I_C}{\partial \beta} \Big| I_{C_0} \& V_{BE} \text{ constant}$$

General Expression for Stability factor S.

$$I_C = \beta I_B + (\beta+1) I_{C_0}$$

Differentiate both sides w.r.t I_C

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{C_0}}{\partial I_C}$$

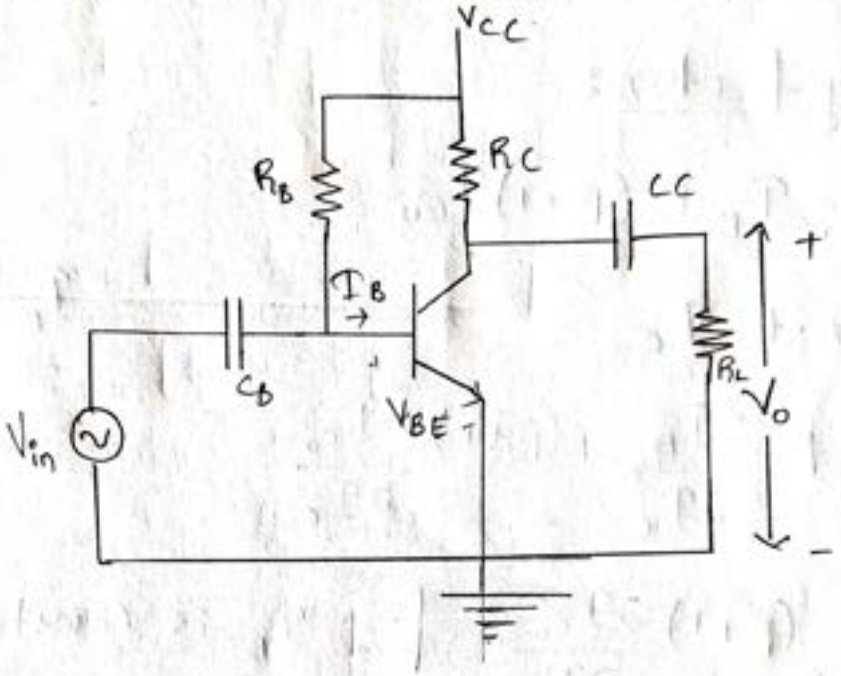
$$(\beta+1) \frac{\partial I_{C_0}}{\partial I_C} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

$$\frac{\partial I_{C_0}}{\partial I_C} = \frac{1 - \beta \frac{\partial I_B}{\partial I_C}}{\beta+1}$$

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{(\beta+1)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

9/3/23 ## Biasing Circuit.

1. Fixed Bias Circuit



It is also known as base-bias circuit. Here the resistance R_B provides a fixed bias voltage to the base. The circuit consist of an npn transistor, collector resistor R_C, base resistor R_B and load resistor R_L. The resistance R_B is selected to obtain the required I_B.

Applying KVL in the i/p side,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B \simeq \frac{V_{CC}}{R_B}$$

$\therefore I_B$ = Constant

This means I_B is a constant and so I_C also constant.

Stability factor:

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

diff w.r.t I_C

I_B = Constant

$\therefore \frac{\partial I_B}{\partial I_C} = 0$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta+1) \frac{\partial I_{CO}}{\partial I_C}$$

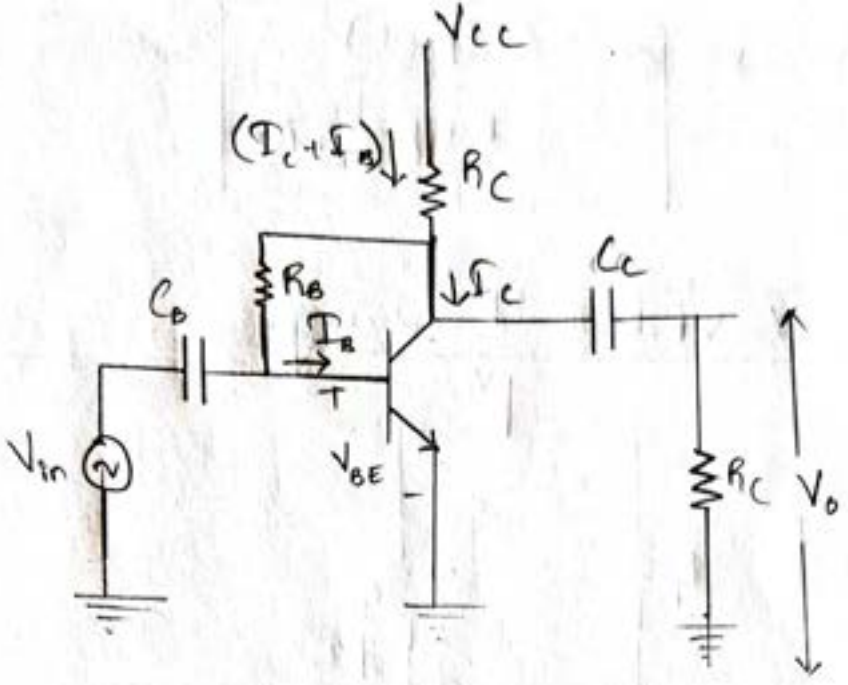
$$1 = (\beta+1) \frac{\partial I_{CO}}{\partial I_C} \quad [\because I_B \text{ is constant}]$$

$$\frac{\partial I_{CO}}{\partial I_C} = \frac{1}{(\beta+1)}$$

$$\therefore \boxed{S = \frac{\partial I_C}{\partial I_{CO}} = (\beta+1)}$$

2. Collector to base [Self] bias circuit.

Here the base bias is provided by R_B. I_C can vary either due to rise in temperature or due to the variation in β. However, increase in I_C decrease I_B which controls I_C. Therefore, Self bias is more stable than fixed bias.



$I_C = \beta I_B$

Stability factor:

Applying KVL in the i/p side,

$$V_{cc} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{cc} - I_C R_C - I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{cc} - I_C R_C - V_{BE} = I_B [R_C + R_B]$$

$$I_B = \frac{1}{R_C + R_B} \left[V_{cc} - I_C R_C - V_{BE} \right]$$

Diff w.r.t I_C,

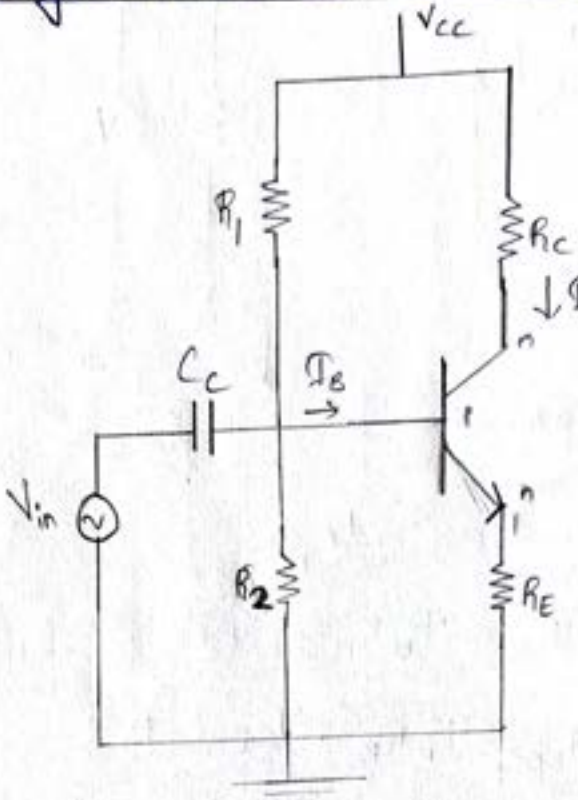
$$\frac{\partial I_B}{\partial I_C} = \frac{1}{R_C + R_B} \left[\frac{\partial V_{cc}}{\partial I_C} - R_C - \frac{\partial V_{BE}}{\partial I_C} \right]$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B} \quad [\because V_{BE} \text{ and } V_{CE} \text{ are constant}] \quad \text{---} (1)$$

$$S = \frac{(\beta + 1)}{1 - \beta \frac{\partial I_B}{\partial I_C}} \quad \text{---} (2)$$

① in ② → $$S = \frac{(\beta+1)}{1+\beta\frac{R_C}{R_C+R_B}}$$

3. Voltage Divider Biasing.

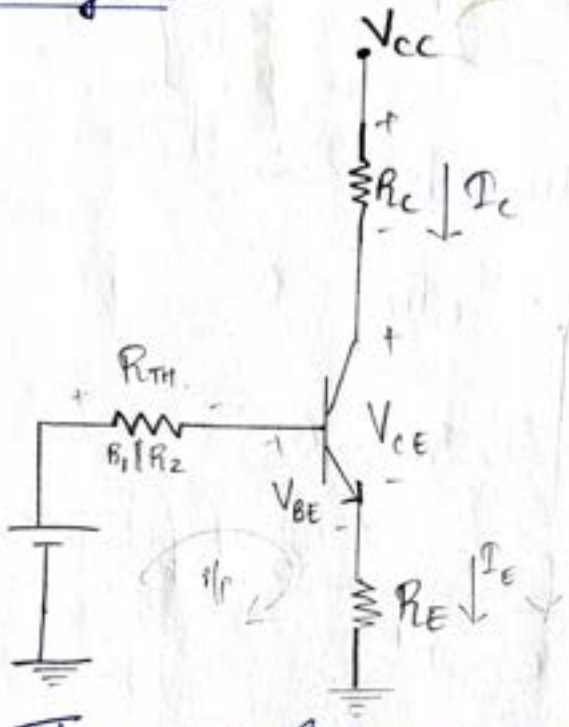


$I_E = I_C + I_B$

This circuit is used when the collector resistance R_C is very small. The current in emitter resistance, R_E causes the voltage drop which is in the direction to reverse bias the emitter base junction. For the transistor to remain in active region, emitter-base jn has to be forward biased. The required bias is obtained from the power supply through the voltage divider n/w R_1 and R_2. If I_C tends to increase due to the increase in I_{CO} with temperature the voltage drop across R_E increases

and thereby decreasing the base current and I_C maintain almost constant.

Analysis:



$I_E = I_C + I_B$

$= \beta I_B + I_B$

$= (\beta+1) I_B$

$I_E = (\beta+1) I_B$

$I_C = \beta I_B$

Thevenin Equivalent circuit.

$$V_{TH} = V_{CC} \times \frac{R_2}{R_1 + R_2} \qquad R_{TH} = R_1 \| R_2$$

Applying KVL at the i/p side,

$$V_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0$$

$$V_{TH} - I_B R_{TH} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$V_{TH} - V_{BE} = I_B R_{TH} + (\beta+1) I_B R_E$$

$\beta+1 \simeq \beta$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta+1) R_E}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + \beta R_E}$$

$$\therefore I_C = \beta \left[\frac{V_{TH} - V_{BE}}{R_{TH} + \beta R_E} \right]$$

I_B

$$= \frac{\cancel{\beta}\,(V_{TH} - V_{BE})}{\cancel{\beta}\left(R_E + \frac{R_{TH}}{\beta}\right)}$$

$R_E >> \frac{R_{TH}}{\beta}$

$\therefore \frac{R_{TH}}{\beta}$ neglected

$$I_C = \frac{V_{TH} - V_{BE}}{R_E} \quad \text{---} (1) \quad \left[R_E >> \frac{R_{TH}}{\beta}\right]$$

Almost $I_E = I_C$ as I_B is minute [since $I_E = I_C + I_B$]

Applying KVL at the o/p side,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \quad \text{---} (2)$$

$\therefore I_C$ independent of β

Stability factor:

$$S = \frac{\partial I_C}{\partial I_{C_0}} = \frac{(\beta + 1)}{1 - \beta \frac{\partial I_B}{\partial I_C}} \quad \text{---} (1)$$

Applying KVL at i/p side,

$$V_{TH} - I_B R_{TH} - V_{BE} - (I_C + I_B) R_E = 0$$

$$V_{TH} - I_B R_{TH} - V_{BE} - I_C R_E - I_B R_E = 0$$

$$I_B = \frac{V_{TH} - V_{BE} - I_C R_E}{R_E + R_{TH}}$$

Diff w.r.t I_C

Constant

$$\frac{V_{TH} - V_{BE}}{R_E + R_{TH}} - \frac{I_C R_E}{R_E + R_{TH}}$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_E + R_{TH}} \quad \text{---} (2)$$

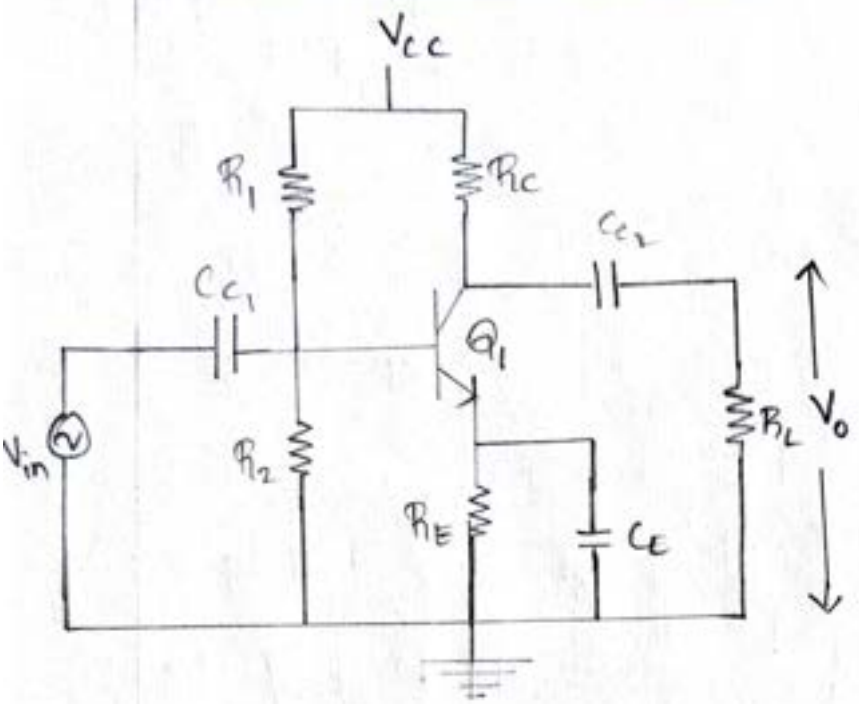
Eqn ② in ①

$$S = \frac{(\beta + 1)}{1 + \beta \frac{R_E}{R_E + R_{TH}}}$$

10/3/23 MODULE - II

MODULE II
BJT AMPLIFIERS

RC Coupled Amplifier.



It is a common emitter amplifier used in audio frequency application amplification for the proper functioning of ~~amplification~~ amplifier transistor must be in active region where the base current has complete control over the collector current ie; $I_c = \beta I_B$

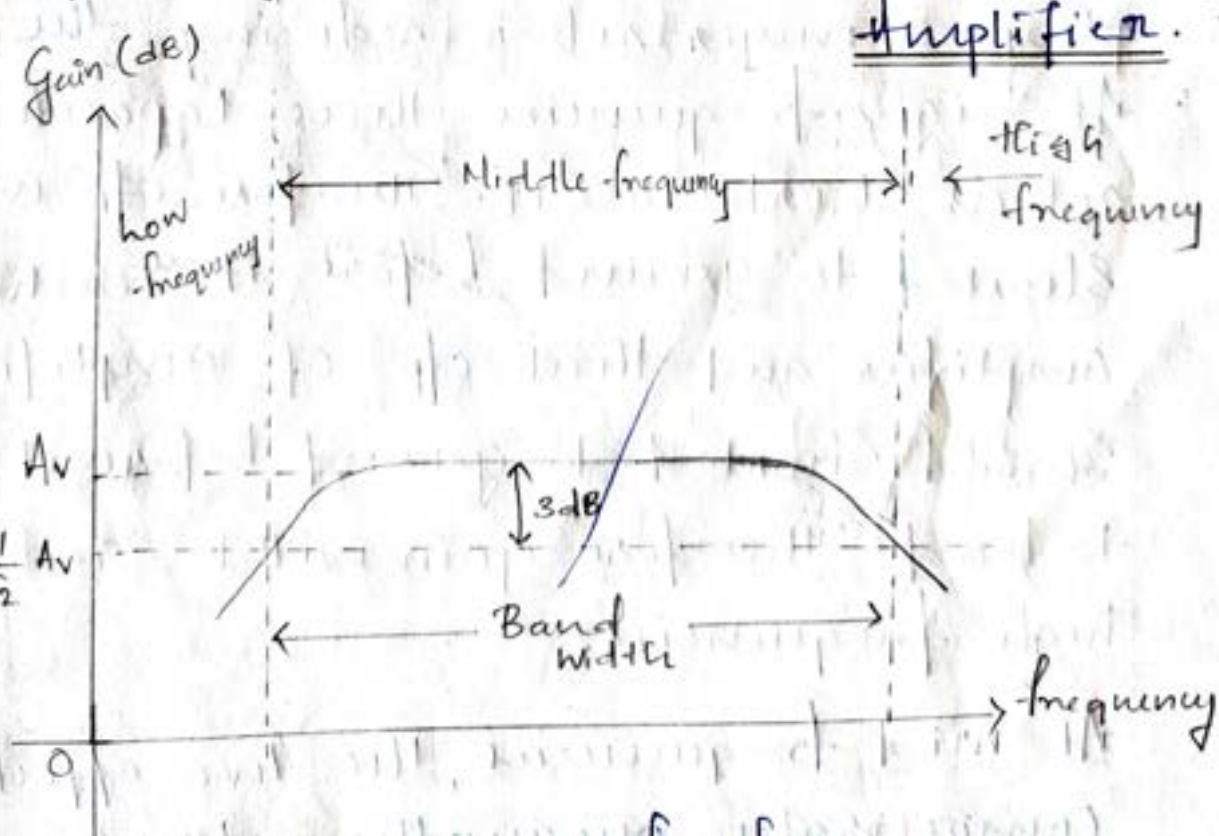
It is a voltage amplifier & the coupling b/w different stages are done by resistance-capacitance coupling. for biasing a voltage divider n/w is used in the circuit.

Here R_1 and R_2 makes a potential divider which is connected across V_{cc} and ground and act as biasing circuit.

C_{C_1} and C_{C_2} are coupling capacitors which blocks the DC component from one stage to another. C_{C_1} couples input signal to the base of amplifier. C_{C_2} is used to block DC component of o/p voltage from reaching the load R_L. R_E stabilizes the operating point against temperature variation. R_C and R_L are acting as a load for the amplifier C_E is the bypass capacitor which bypasses the AC signal developed across R_E to ground. The reactance of C_E should be much less than R_E i.e;

$$X_{CE} \leq \frac{R_E}{10}$$

Frequency Response of RC coupled Amplifier.



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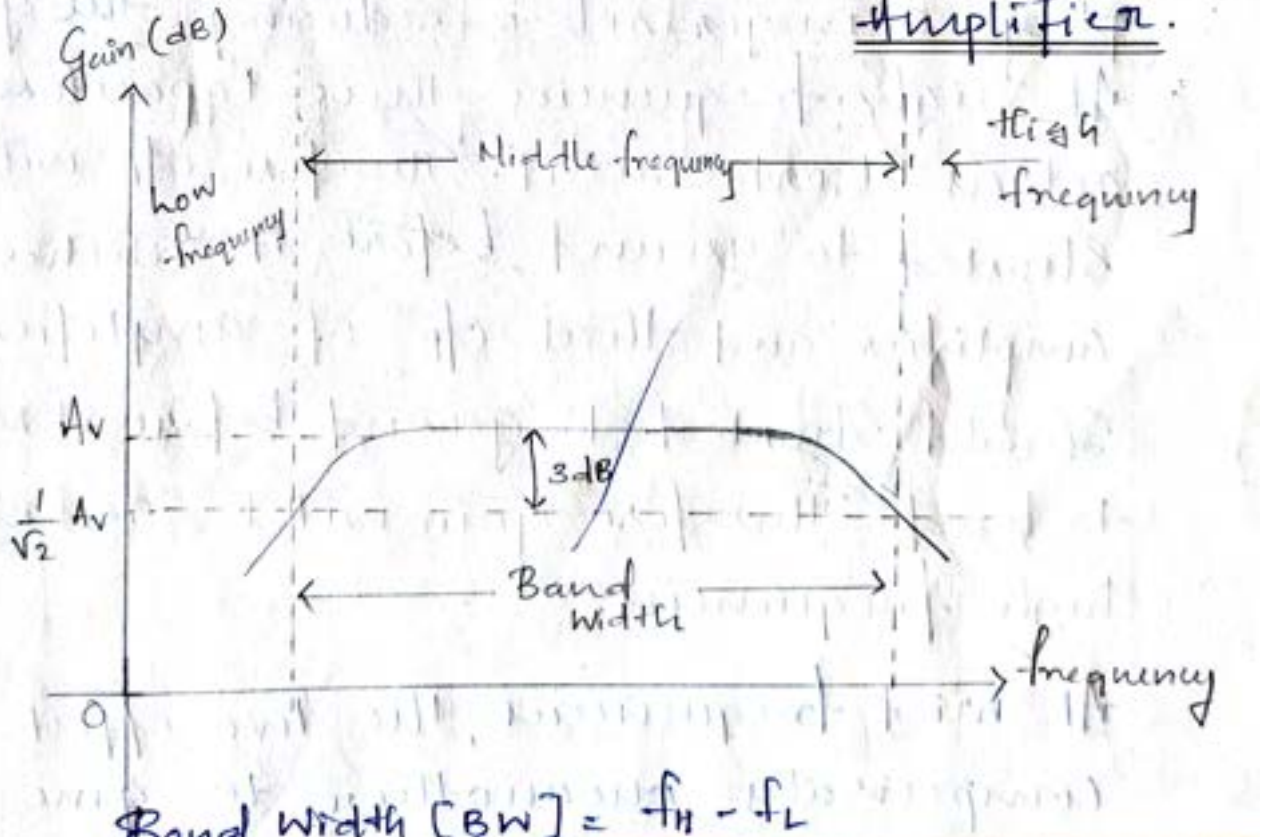
Frequency Response of RC coupled Amplifier.



Band Width [BW] = $f_H - f_L$

In the frequency response plot we can see the gain roll off and low and high frequency ranges. and constant gain at mid frequencies.

At low frequencies:

At low frequencies the reactance of coupling capacitors C_1 and C_2 will be very high $\left[X_c = \frac{1}{2\pi fC}\right]$ and therefore i/p signal voltage will not couple properly to amplifier and the amplified o/p will not couple properly to load. Therefore gain reduces on low frequencies.

At high frequencies:

At high frequencies, inter electrode capacitances and stray wiring capacitore's plays a major role in reducing the gain. At high frequencies these capacitors will act as short circuit. Therefore o/p will be shorted to ground before it reaches the amplifier and that o/p of amplifier also should shorted to ground before it reaches to load. Therefore gain will be reduced at high frequencies.

At mid frequencies, the two effects compensates oneanother to give

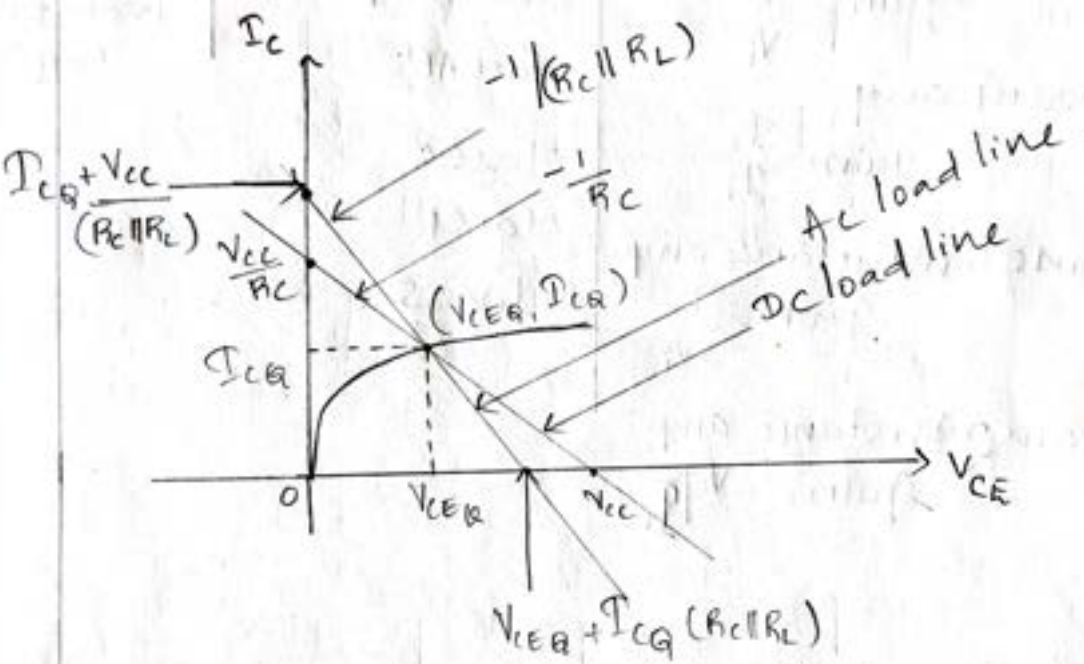
constant gain.

Here the Bandwidth of an amplifier is defined as the range of frequencies over which the amplifier provides desired gain.

$$BW = f_H - f_L$$

10/3/23

Ac load line.



Classification of Amplifiers.

Amplifiers

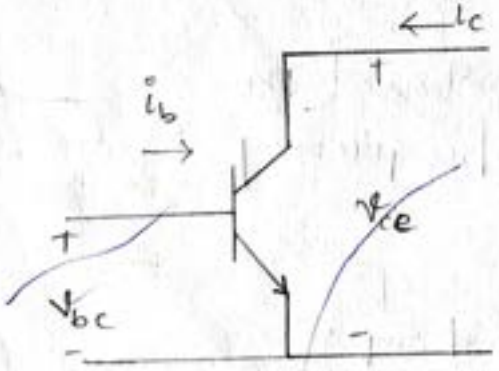
- Based on i/p and o/p
  - Small Signal amp
    - Voltage amp, gain = $\frac{V_o}{V_i}$
    - Current amp, gain = I_o/I_i
    - Trans Conductance amp, gain = $\frac{I_o}{V_i}$
    - Trans resistance amp, gain = $\frac{V_o}{I_i}$
  - Large Signal amp
- Based on frequency
- Based on Coupling

Amplifiers

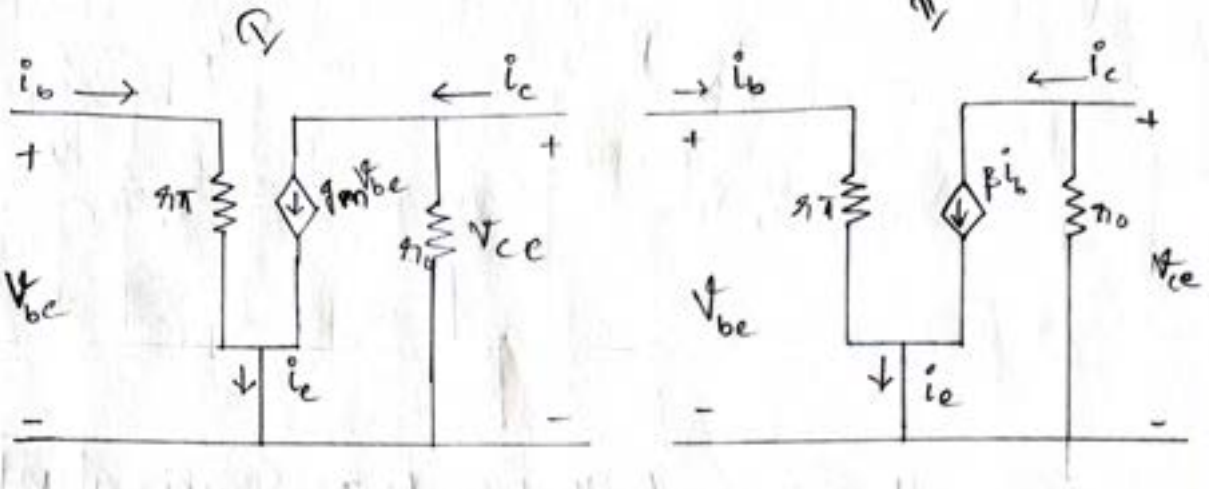
- Based on i/p used o/p
  - Small Signal amplifiers
    - Voltage amplifiers, Gain = $\frac{V_o}{V_i}$
    - Current amp, Gain = $\frac{I_o}{I_i}$
    - Trans conductance amp, Gain = $\frac{I_o}{V_i}$
    - Transresistance amp, Gain = $\frac{V_o}{I_i}$
  - Large Signal amplifiers
    - Class A
    - Class B
    - Class AB
    - Class C
    - Class D
    - Class S
- Based on frequency
  - Audio freq amp
  - Radio freq amp
- Based on Coupling
  - RC coupling
  - LC coupling
  - Direct coupling
  - Transformer coupling

Small Signal Model of BJT

Small Signal Hybrid-π model



MODEL:



Input resistance/ Impedance $r_\pi = \frac{v_{be}}{i_b} = \frac{V_T}{I_{BQ}} = \frac{I_{CQ}}{\beta}$ — thermal equivalent $V_{qe} = 26mV$

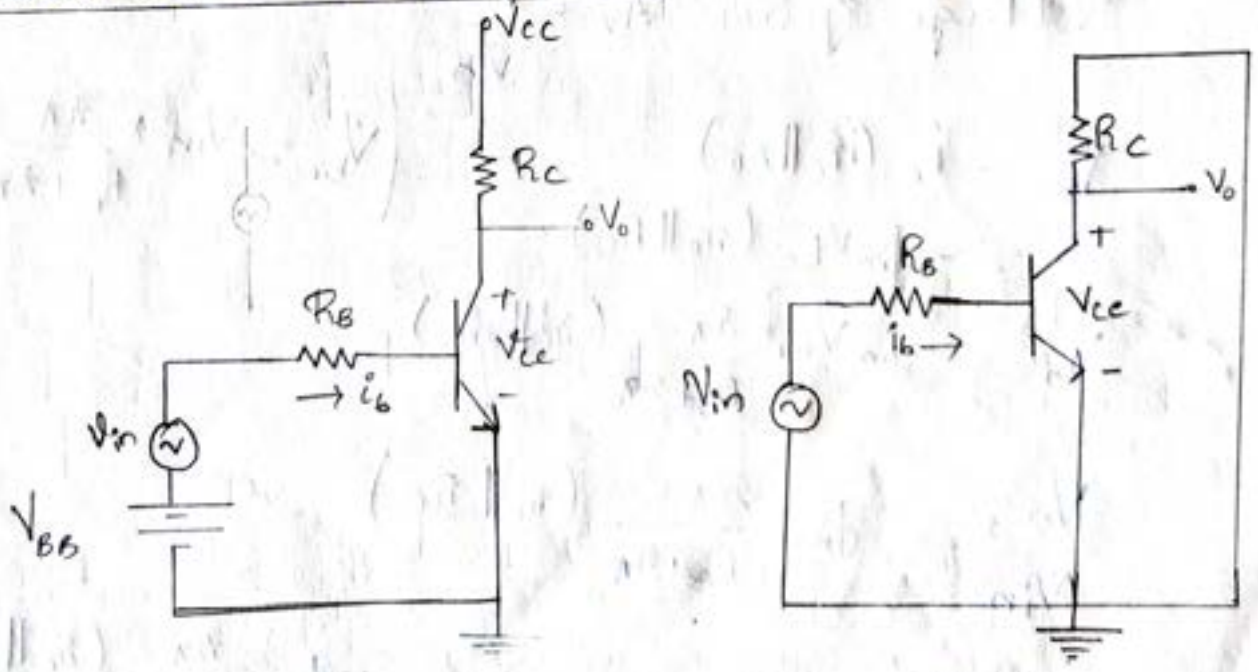
$$= \frac{\beta V_T}{I_{CQ}}$$

g_m = transconductance $= \frac{i_c}{v_{be}}$

Output resistance, $r_o = \frac{v_{ce}}{i_c} = \frac{V_A}{i_c}$

V_A = Early voltage

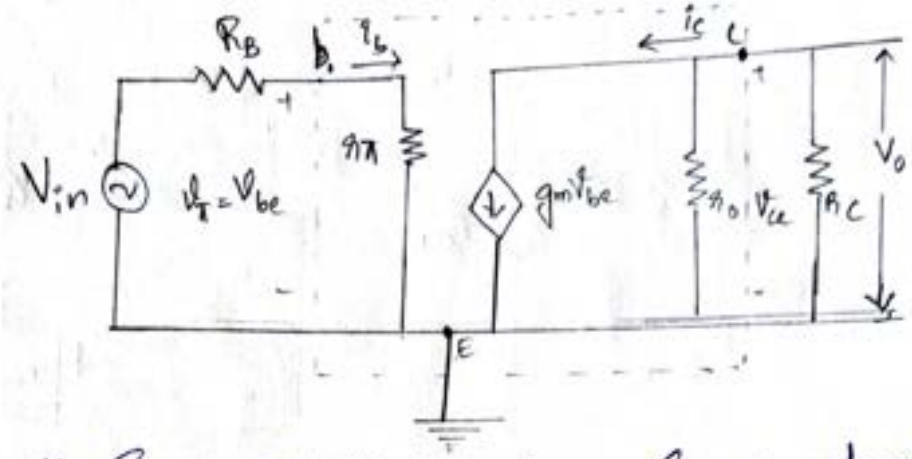
Common Emitter Circuit [CE ckt]



DC

AC Equivalent

AC Small Signal Model



Small Signal Hybrid-π Equivalent circuit of Common-Emitter Stage.

Common-Emitter Current gain.

$$i_c = g_m V_{be} \qquad i_b = V_{be} / r_\pi$$

$$\therefore \frac{i_c}{i_b} = \frac{g_m V_{be}}{V_{be}/r_\pi} = g_m r_\pi$$

Current gain, $\frac{i_c}{i_b} = g_m r_\pi$

Voltage gain, $A_V = \frac{V_o}{V_{in}}$

$$V_o = -i_c (R_C \| r_o) \qquad \left[V_{be} = V_{in} \times \frac{r_\pi}{R_B + r_\pi} \right]$$

$$= -g_m V_{be} (r_o \| R_C)$$

$$V_o = -g_m V_{in} \times \frac{r_\pi}{R_B + r_\pi} (r_o \| R_C)$$

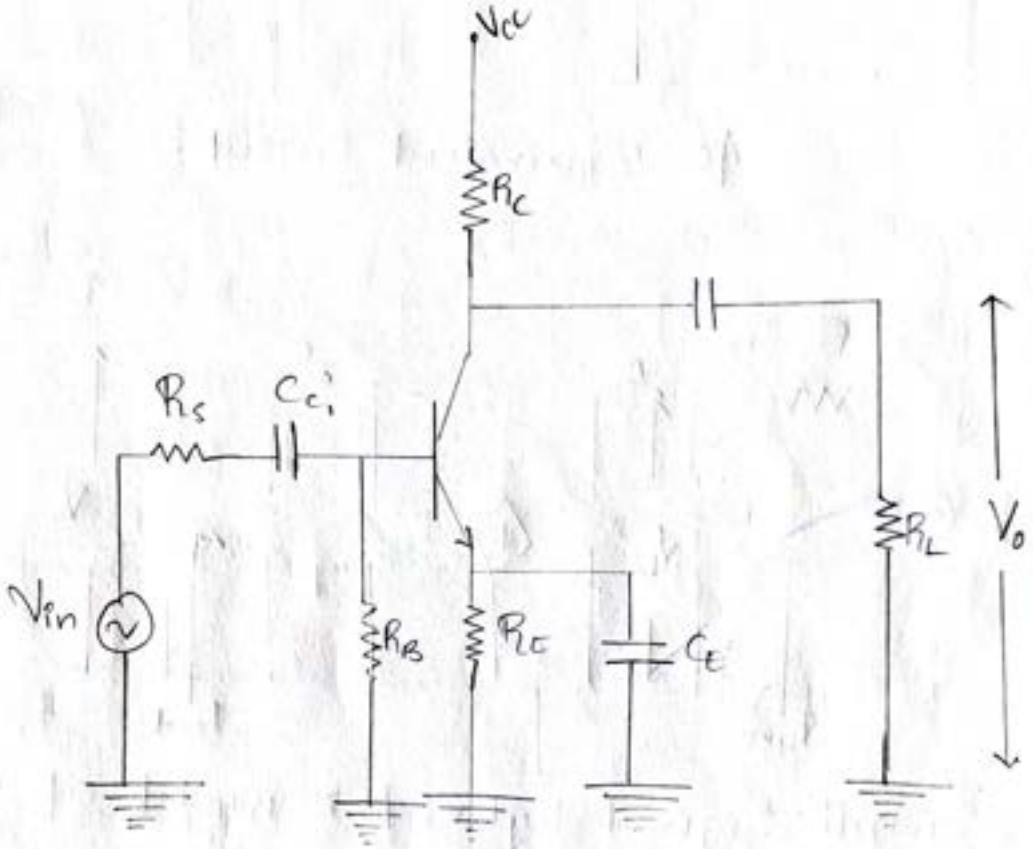
$$\frac{V_o}{V_{in}} = -g_m \frac{r_\pi}{R_B + r_\pi} (r_o \| R_C)$$

$\therefore$ Voltage gain $A_{V_1} = \frac{V_o}{V_{in}} = -g_m \frac{r_\pi}{R_B + r_\pi} (r_o \| R_C)$

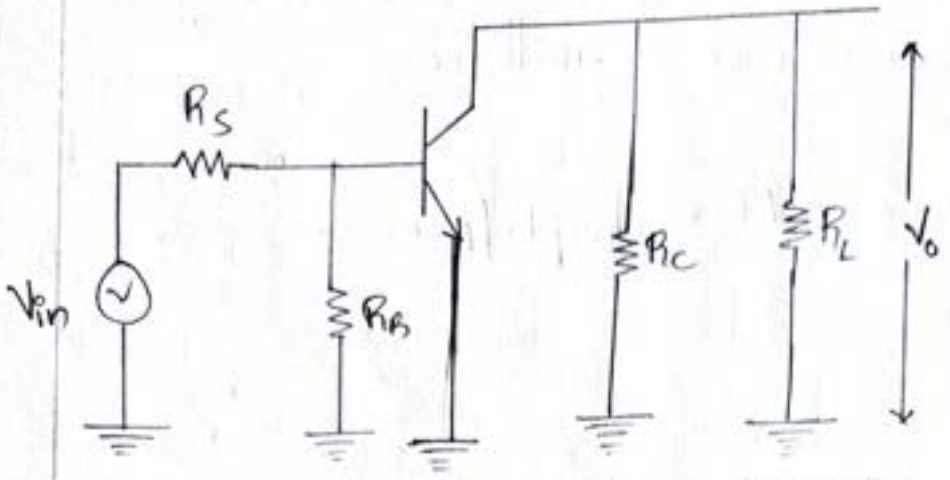
Input impedance = $r_\pi \parallel R_B$

Output impedance = $r_o \parallel R_C$

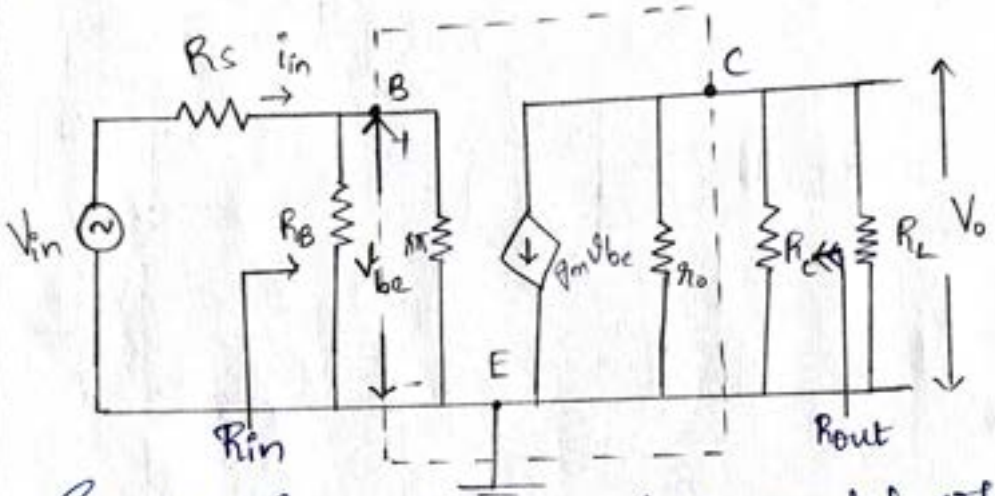
Common-Emitter Amplifier.



The common-Emitter configuration is the most widely used for all BJT amplifier circuits. Here, the emitter bypass capacitor C_E is connected b/w emitter and ground. This capacitor is required to provide a very low impedance to ground. To determine the terminal characteristics of C_E amplifier i.e, its i/p impedance, o/p impedance and voltage gain replaced the BJT with its hybrid by small signal model.



Ac Equivalent Circuit.



Small Signal hybrid-π model of CE circuit.

Input Impedance:

$$R_{in} = \frac{V_{in}}{i_{in}} = R_B \| r_\pi$$

Output Impedance:

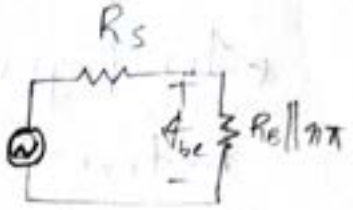
$R_{out} = r_o \| R_C$, if R_L is included, then $\Rightarrow R_{out} = r_o \| R_C \| R_L$

Voltage Gain:

$$A_V = \frac{V_{out}}{V_{in}} \quad \longleftarrow (1)$$

$V_{out} = -g_m V_{be} (r_o \| R_C \| R_L)$ ——— (2)

$V_{be} = V_i \dfrac{(R_B \| r_\pi)}{R_S + (R_B + R_\pi)}$ ——— (3)



Substitute (3) in (2)

$$V_{out} = -g_m V_i \frac{(R_B \| r_\pi)}{R_S + (R_B \| r_\pi)} (r_o \| R_C \| R_L)$$

$$\frac{V_{out}}{V_{in}} = -g_m \frac{(R_B \| r_\pi)}{R_S + (R_B \| r_\pi)} (r_o \| R_C \| R_L)$$

$$\therefore A_V = \frac{V_{out}}{V_{in}} = -g_m \frac{(R_B \| r_\pi)}{R_S + (R_B \| r_\pi)} (r_o \| R_C \| R_L)$$

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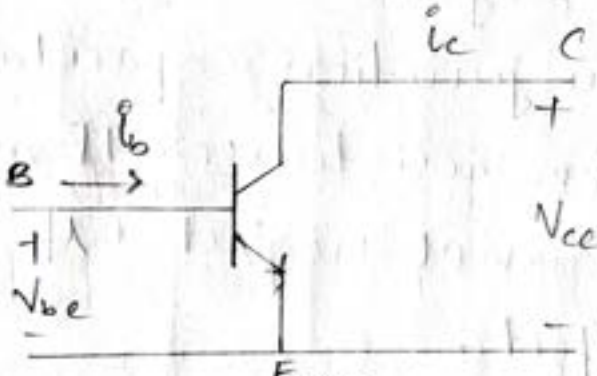
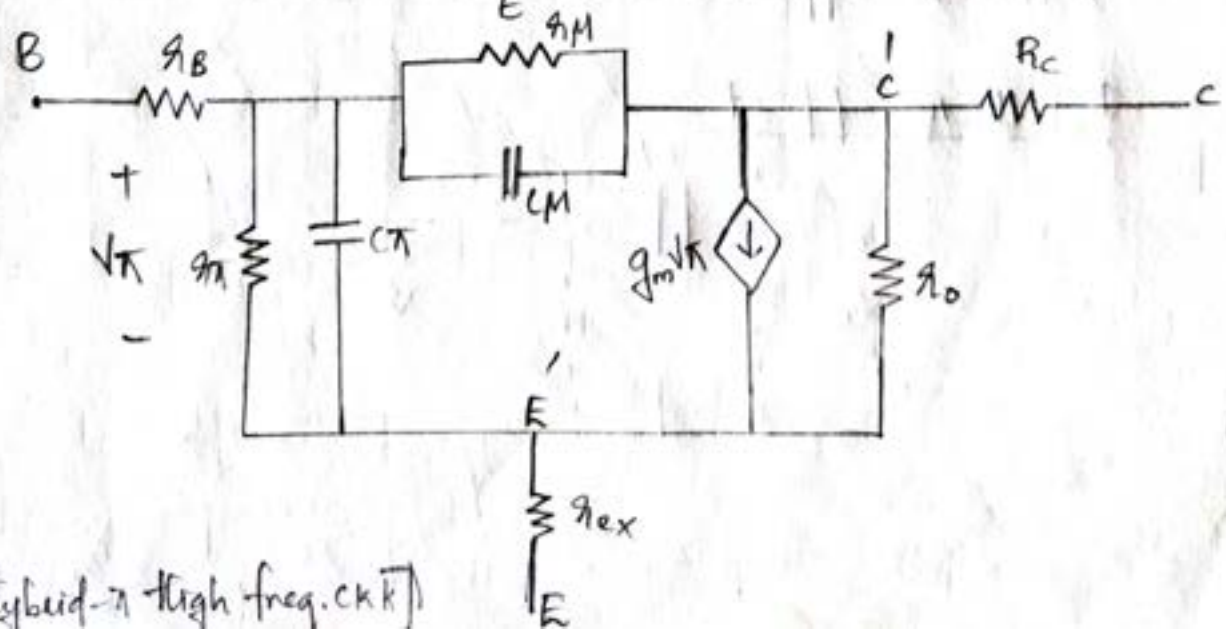
Hybrid π Equivalent Circuit [High Frequency].



Common-Emitter npn transistor with small signal voltage & current

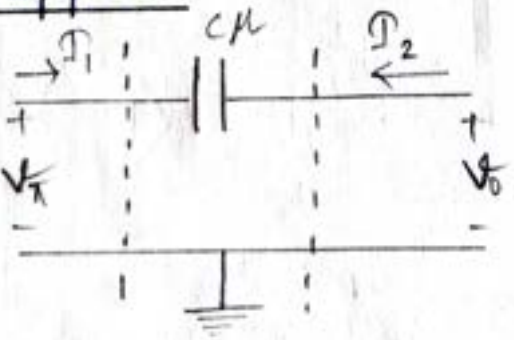


[Hybrid-π High freq. ckt]

~~High~~ High frequency hybrid Model.

* In figure r_B is the base series resistance between external base terminal and internal base terminal.
* B' - E' is the forward biased junction and so r_π and C_π are the forward biased jn resistance and capacitance respectively.
* r_{ex} is the emitter series resistance b/w external and internal emitter terminals.
* r_c is the resistance b/w external and internal collector terminals.
* $g_m V_\pi$ - Voltage controlled current source.
* r_o is the inverse of o/p conductance g_o.
* Since B' - C' junction is reverse biased, C_μ is the junction capacitance and r_μ is the junction resistance. Here $C_\mu \ll C_\pi$ but we cannot neglect C_μ (feedback capacitance) because of Miller Effect.

Miller Effect.

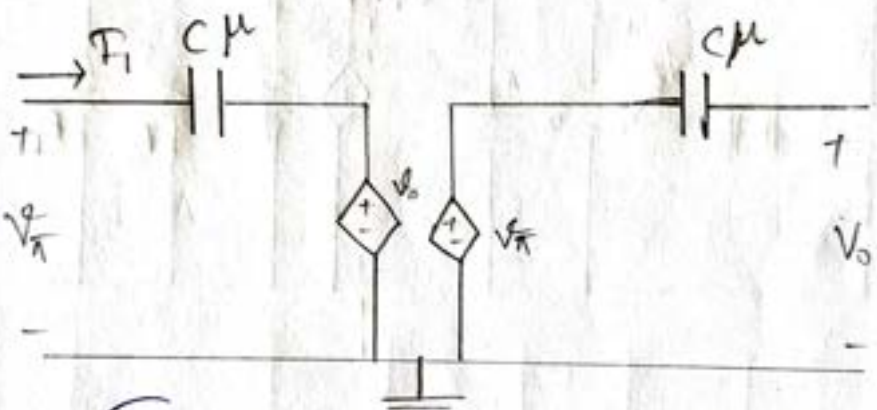


The Miller Effect is the multiplication effect of feedback capacitance C_M in circuit applications. In figure, by applying KVL, in the i/p side,

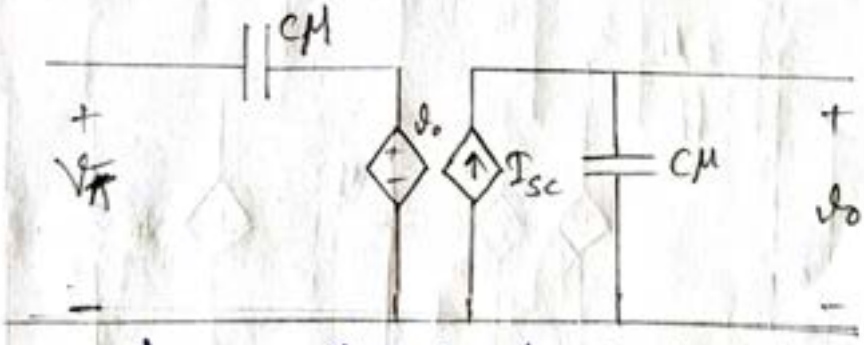
$$V_\pi = I_1 \left[\frac{1}{j2\pi f C_M} \right] + V_o \quad \text{——— (1)}$$

and by applying KVL, in the o/p side,

$$V_o = I_2 \left[\frac{1}{j2\pi f C_M} \right] + V_\pi \quad \text{——— (2)}$$

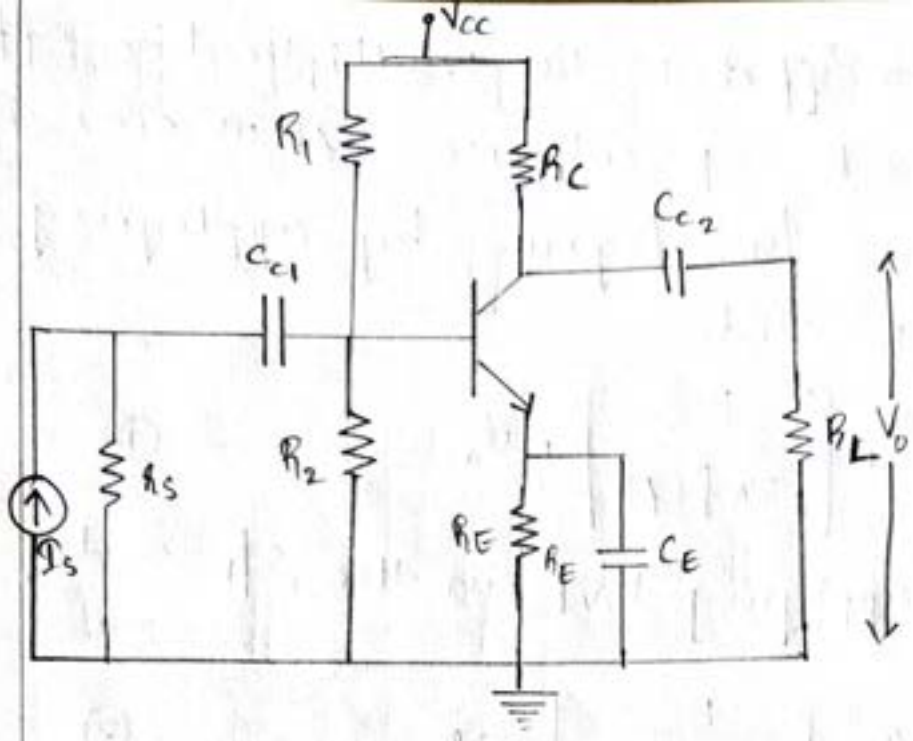


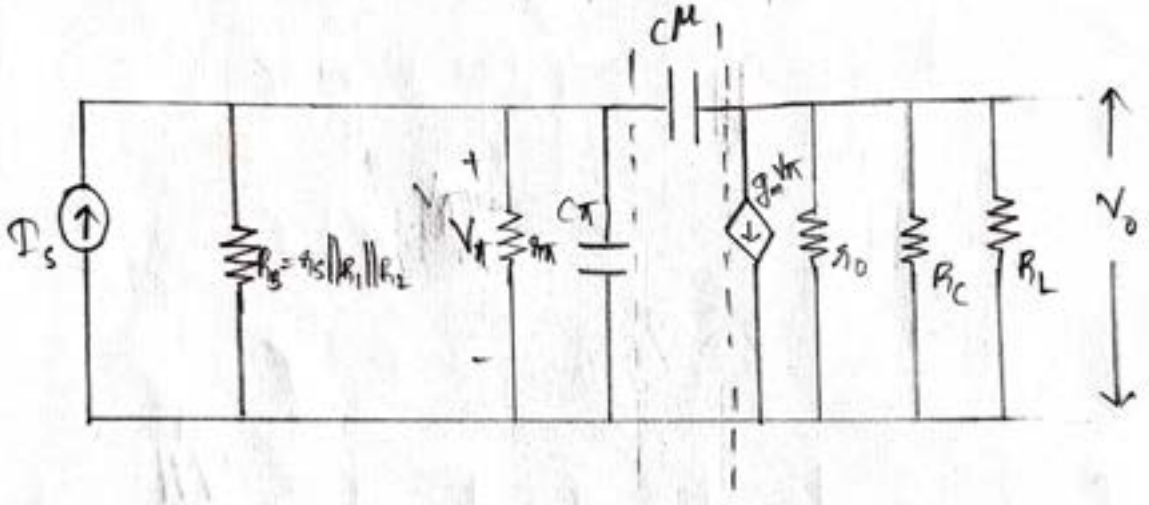
Thevenin Equivalent Circuit.

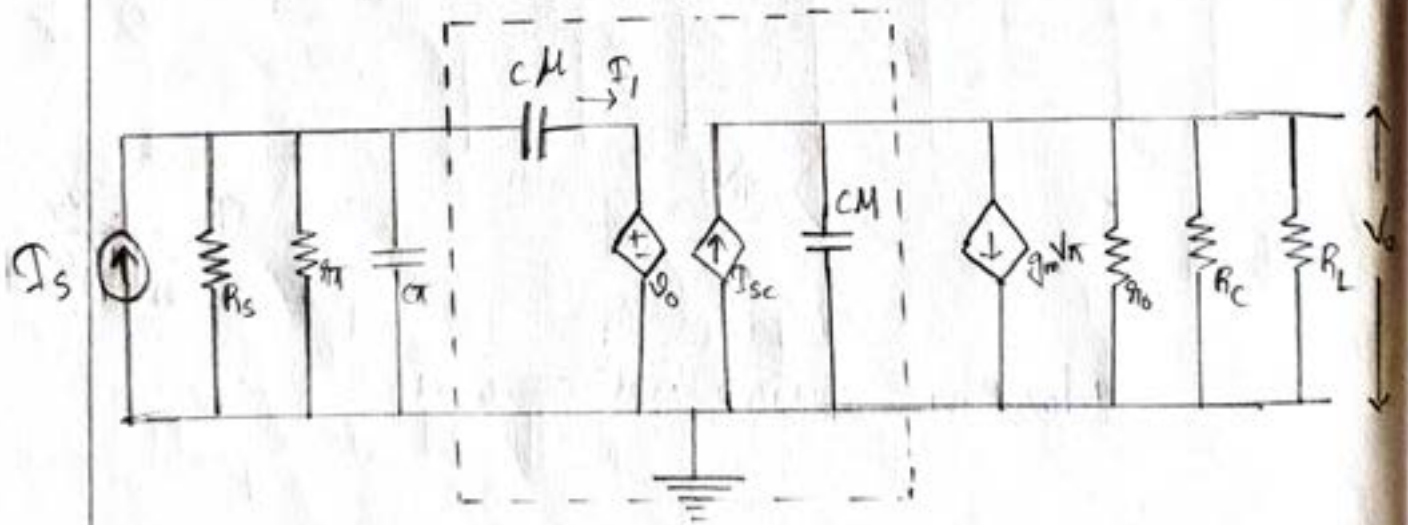


Norton Equivalent circuit

$$I_{sc} = \frac{V_\pi}{1/j2\pi f_c}$$







We can neglect I_{sc}, because ~~it is~~ $I_{sc} << g_m V_\pi$.
When the impedance of $C_M = R_C \| R_L$

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$$\frac{1}{\omega C_M} = R_C \parallel R_L \qquad f = \frac{1}{2\pi (R_C \parallel R_L) C_M}$$

$$\frac{1}{2\pi f C_M} = R_C \parallel R_L$$

$$I_1 = \frac{V_\pi - V_o}{1/j\omega C_M} = j\omega C_M (V_\pi - V_o) \longrightarrow (1)$$

$$V_o = -g_m V_\pi (r_o \parallel R_C \parallel R_L) \longrightarrow (2)$$

Substitute (2) in (1)

$$I_1 = j\omega C_M \{ V_\pi + g_m V_\pi (r_o \parallel R_C \parallel R_L) \}$$

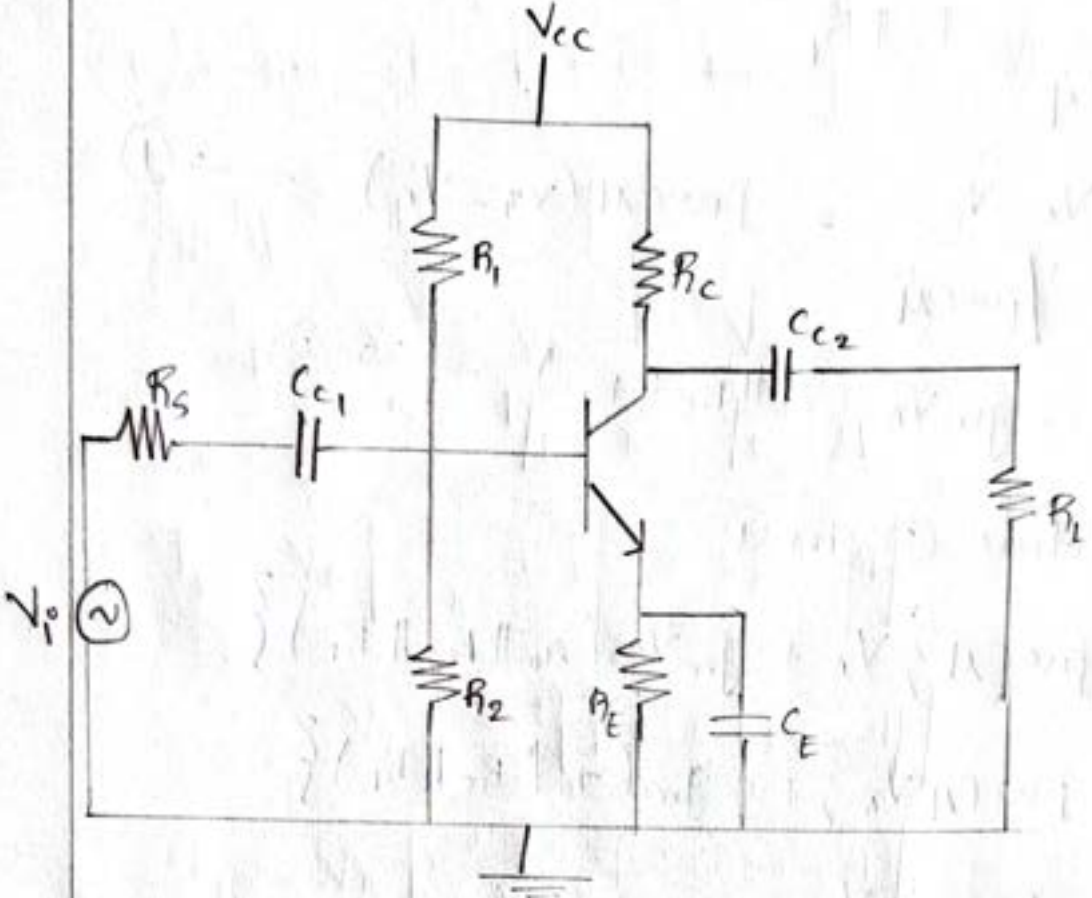
$$I_1 = j\omega C_M V_\pi \{ 1 + g_m (r_o \parallel R_C \parallel R_L) \}$$

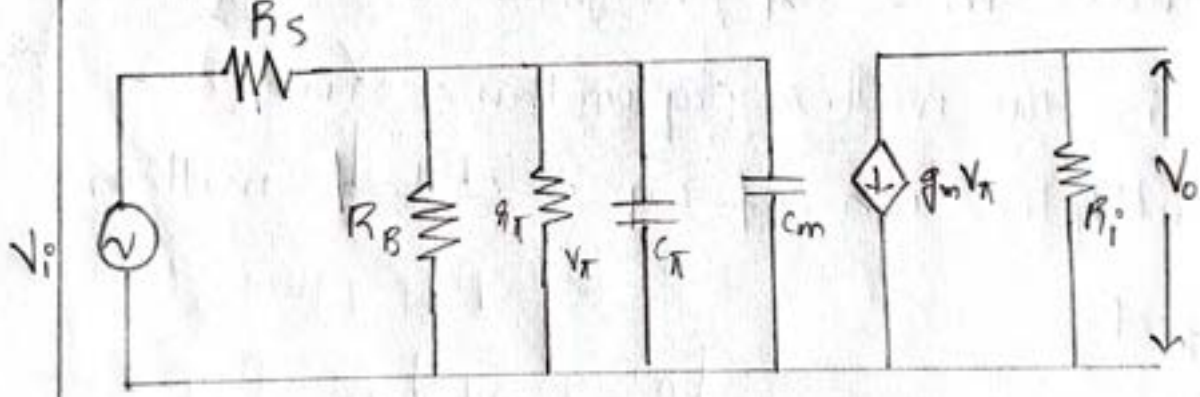
$$I_1 = j\omega C_m V_\pi \longrightarrow (3)$$

Where $C_m = C_M \{ 1 + g_m (r_o \parallel R_C \parallel R_L) \}$

C_M is the miller capacitance and multiplication of C_M is called miller effect.

Higher-frequency Response of CE Amplifier.





$$f_H = \frac{1}{2\pi \tau_p} = \frac{1}{2\pi R_{eq} \cdot C_{eq}}$$

$$R_{eq} = R_S \| R_B \| r_\pi$$

$$R_{eq} = R_S \| R_B \| r_\pi$$

$$C_{eq} = (C_M + C_\pi)$$

The high frequency equivalent circuit includes the Miller capacitance C_M.

$$C_M = C_\mu \left[1 + g_m (r_o \| R_C \| R_L)\right]$$

The upper 3dB frequency,

$$f_H = \frac{1}{2\pi (R_S \| R_B \| r_\pi)(C_\pi + C_M)}$$

To find the mid-band gain we assume C_π and C_M as open.

Voltage gain, $A_V = \frac{V_o}{V_i}$

$$V_o = -g_m V_\pi R_L$$

Here V_π in terms of V_i is,

$$V_\pi = V_i \times \frac{(R_B \| r_\pi)}{R_S + (R_B \| r_\pi)}$$

$$\therefore V_o = -g_m V_i \left[\frac{(R_B \| r_\pi)}{R_S + (R_B \| r_\pi)}\right] R_L'$$

$$\boxed{A_V = \frac{V_o}{V_i} = -g_m \left[\frac{R_B \| r_\pi}{R_S + (R_B \| r_\pi)}\right] R_L'}$$

~~Here~~ ~~V_π~~

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SHORT CIRCUIT CURRENT GAIN

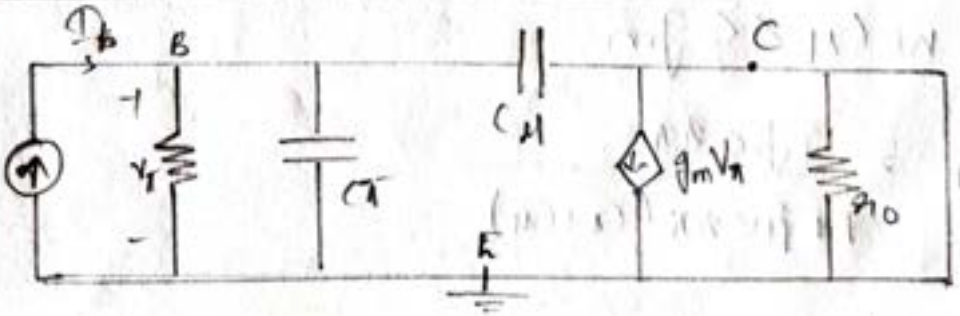


figure shows simplified hybrid π model for transistor after neglecting r_b, r_c, r_{ext}, r_M and C_S. The short current gain $AI = \frac{I_c}{I_b}$.

Apply KCL at i/p side;

$$I_b = \frac{V_\pi}{r_\pi} + \frac{V_\pi}{1/j\omega C_\pi} + \frac{V_\pi}{1/j\omega C_M}$$

$$I_b = V_\pi \left[\frac{1}{r_\pi} + j\omega C_\pi + j\omega C_M\right].$$

$$= V_\pi \left[\frac{1}{r_\pi} + [j\omega C_\pi + j\omega C_M]\right]$$

$$I_b = V_\pi \left[\frac{1}{r_\pi} + j\omega (C_\pi + C_M)\right] \quad \text{—— ①}$$

Apply KCL at the o/p side;

$$I_c + \frac{V_\pi}{1/j\omega C_M} = g_m V_\pi$$

$$I_c + V_\pi j\omega C_M = g_m V_\pi$$

$$I_c = V_\pi [g_m - j\omega C_M] \quad \text{—— ②}$$

$$A_i = \frac{I_c}{I_b} = \frac{(g_m - j\omega C_M)}{1/r_\pi + j\omega (C_\pi + C_M)} = \frac{(g_m - j\omega C_M) r_\pi}{1 + j\omega r_\pi (C_\pi + C_M)}$$

$\because \omega C_M << g_m$

$$A_i = \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_M)}$$

let $g_m r_\pi = \beta$

$$\frac{1}{2\pi r_\pi (C_\pi + C_\mu)} = \omega_\beta$$

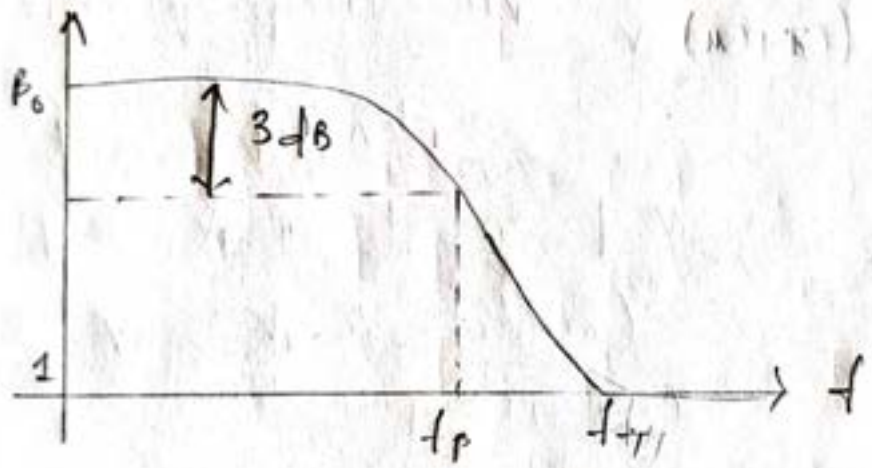
$$A_i = \frac{\beta}{1 + j\omega r_\pi (C_\pi + C_\mu)}$$

$$2\pi f_\beta = \frac{1}{r_\pi (C_\pi + C_\mu)}$$

$$A_i = h_{fc} = \frac{\beta}{1 + j(\omega/\omega_\beta)}$$

$$f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)}$$

$$|h_{fc}| = \frac{\beta}{\sqrt{1 + (f/f_\beta)^2}}$$



Here f_T is the frequency at which the short circuit current gain = unity (unity gain bandwidth)

$$\boxed{|h_{fc}| = \frac{\beta}{\sqrt{1 + (f/f_\beta)^2}}}$$

$$1 = \frac{\beta}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}}$$

$$1 \simeq \frac{\beta}{f_T/f_\beta}$$

$$\frac{f_T}{f_\beta} = \beta$$

$$f_T = \beta \cdot f_\beta$$

$$f_T = \beta \frac{1}{2\pi r_\pi (C_\pi + C_\mu)}$$

$$\boxed{f_T = \frac{\beta}{2\pi r_\pi (C_\pi + C_\mu)}}$$

$$f_T = \frac{g_m r_\pi}{2\pi r_\pi (C_\pi + C_\mu)} = \frac{g_m}{2\pi (C_\mu + C_\pi)}$$

$$f_T = \frac{g_m}{2\pi (C_\pi + C_\mu)}$$

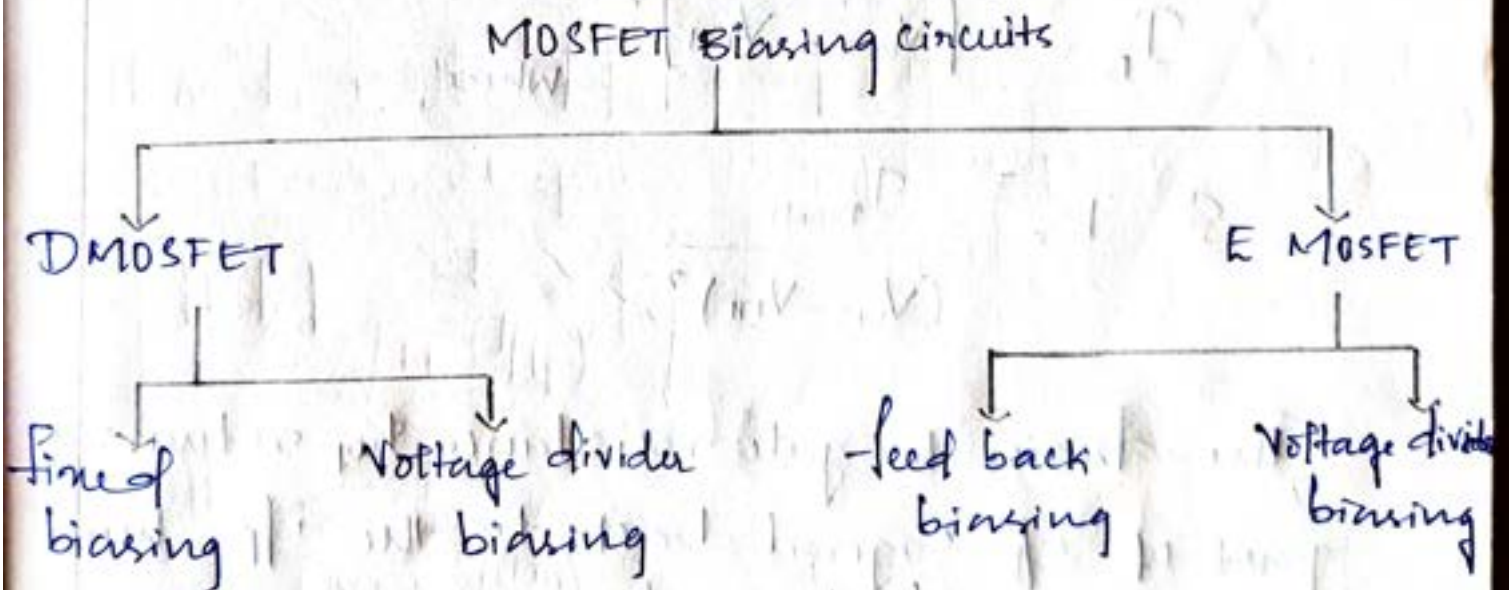
MODULE – III

MOSFET CIRCUITS

MOSFET Biasing:

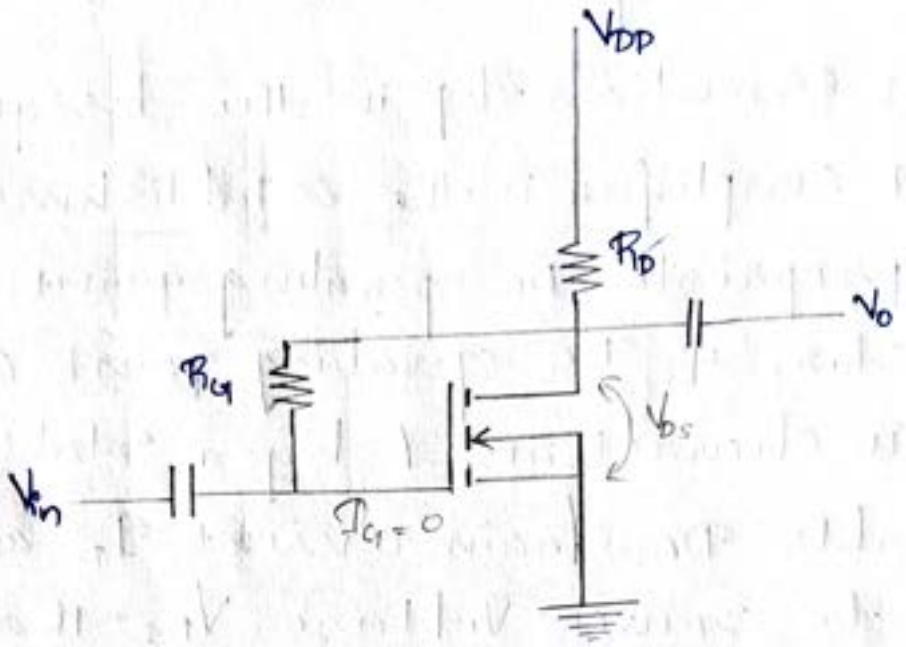
An essential step in the design of MOSFET amplifier is the establishment of an appropriate DC operating point for the transistor. A DC operating point or bias point is characterised by a stable and creditable DC drain current I_D and DC drain to source voltage V_{DS} that ensures the operation in saturation region for all expected i/p signal levels.

MOSFET Biasing Circuits.



E-MOSFET Biasing

1. Feedback biasing circuit.



In an n-channel E-MOSFET the drain current $I_D = 0$ for $V_{GS} < V_{TH}$ and for $V_{GS} > V_{TH}$ the relation between I_D and V_{GS} is given by,

$$I_D = k\left[V_{GS} - V_{TH}\right]^2$$ Where,

$$\text{Ⓕ}\quad k = \frac{I_{D(ON)}}{(V_{GS} - V_{TH})^2}$$

The drain to gate resistance R_G returns a part of o/p signal back to the i/p hence the name feedback biasing. Due to the presence of SiO_2 layer, the i/p impedance is very large.

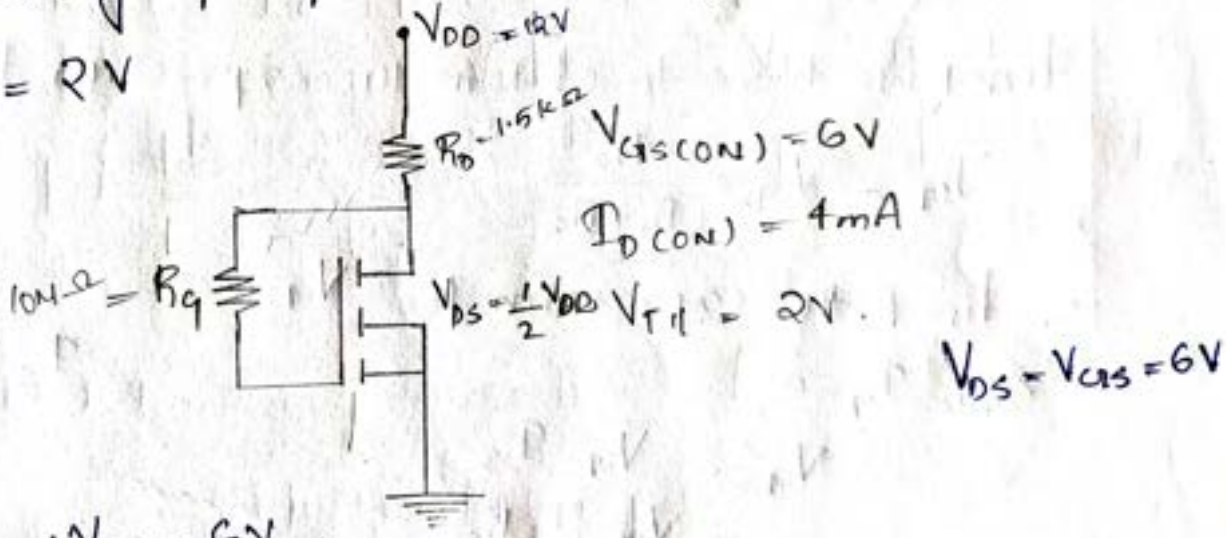
$\therefore I_G = 0$ and $V_{RG} = 0$

So, $V_{DS} = V_{GS}$

For mathematical analysis, values of $I_{D(ON)}$ and $V_{GS(ON)}$ and V_{TH} are provided, we have to calculate I_{DQ} and V_{DSQ}, where

$$\boxed{I_{DQ} = K\left[V_{GS} - V_{TH}\right]^2} \; ; \; \boxed{V_{DSQ} = V_{DD} - I_D R_D}$$

6 Design a feedback biasing circuit for the following specifications. $V_{GS(ON)} = 6V$, $I_{D(ON)} = 1mA$ $V_{TH} = 2V$



$V_{DS} = \frac{1}{2}V_{DD} = 6V$

For a Good amplifiere $V_{DS} = \frac{V_{DD}}{2}$

$\therefore V_{DD} = \underline{12V}$.

Apply KVL in o/p Side;

$V_{DD} - I_D R_D - V_{DS} = 0 \rightarrow 12 - I_D R_D - V_{DS} = 0$

$\therefore R_D = \frac{12-6}{4\times10^{-3}}$ $\therefore R_D = 1.5\times10^3 = \underline{1.5k\Omega}$.

$R_G = 10M\Omega$ [$\because I_G = 0$ and have high i/p impedance we give a high resistance value]

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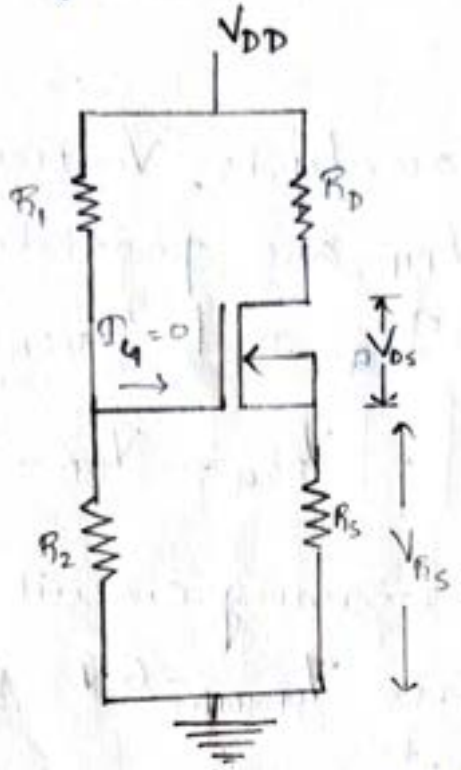
Voltage Divider Biasing.



first, we have to obtain the expression for V_G

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

2. find the expression for V_{GS}

$I_S = I_D$

Since $I_G = 0$;

$$V_{GS} = V_G - I_S$$
$$= V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S$$

3. Calculate the value of I_{D_Q}.

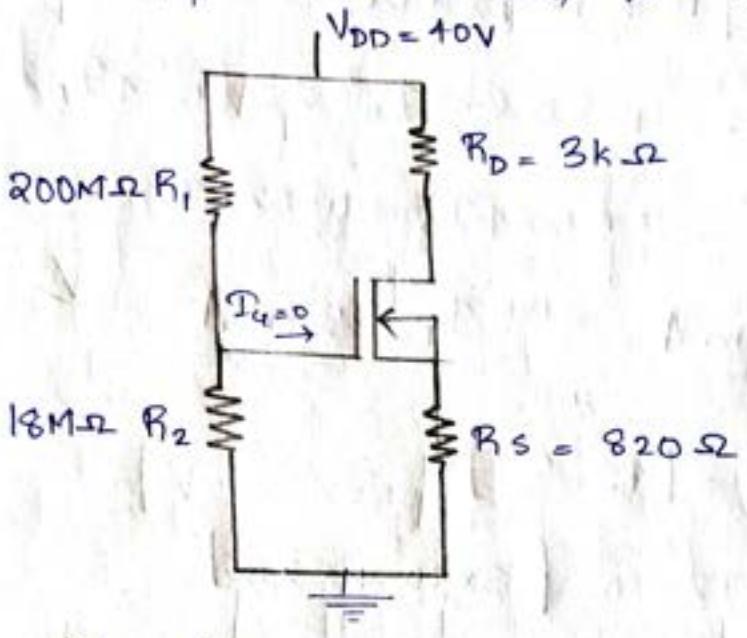
$$I_{D_Q} = K \left[V_{GS} - V_{TH} \right]^2$$

4. find V_{DS_Q}

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D \left[R_D + R_S \right]$$

6 find I_{DQ}, V_{GS} and V_{DSQ} for the given circuit.



$V_{GS} = V_G - V_S$

$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2} \Rightarrow 10 \times \frac{16 \times 10^6}{200 \times 10^6 + 16 \times 10^6}$

$V_G = 18V$.

$V_S = I_D R_S$

$V_{GS} = V_G - I_D R_S = 18 - I_D R_S$ — ①

$I_D = K[V_{GS} - V_{TH}]^2$ — ②

$K = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_{TH}]^2}$ — ③

$= \frac{3 \times 10^{-3}}{(10-5)^2} = \frac{3 \times 10^{-3}}{25}$

$= 120 \times 10^{-6}$

$= 120\mu$

$I_D = 120 \times 10^{-6}[18 - I_D R_S - 5]^2$

$= 120 \times 10^{-6}[13 - I_D R_S]^2$ $(a-b)^2$

$= 120 \times 10^{-6}[169 + I_D^2 R_S^2 - 2 \times 13 \times I_D R_S]$

$= 120\times10^{-6}\left[169 + 672400 I_D^2 - 21320 I_D\right]$

$I_D = 0.02028 + 80.688 I_D^2 - 2.5584 I_D$

$80.688 I_D^2 - 2.5584 I_D + 0.0208$

$I_D = 6.72\,mA$ $\qquad$ $I_D = 37\,mA$

$V_{DS} = V_{DD} - I_D[R_D + R_S]$

$= 40 - 6.72\times10^{-3}\left[3\times10^3 + 820\right]$

$= 40 - 5.494$

$= 14.32.$

$V_{DS} = V_{DD} - 37.4\times10^{-3}\left[3\times10^3 + 820\right]$

$= -102.8.$

$\therefore I_{DQ} = 6.72\,mA$

$V_{DS} = 14.32$

Substitute I_D in ①

$V_{GS} = 18 - \left[6.72\times10^{-3}\times820\right]$

$V_{GS} = 12.46V.$

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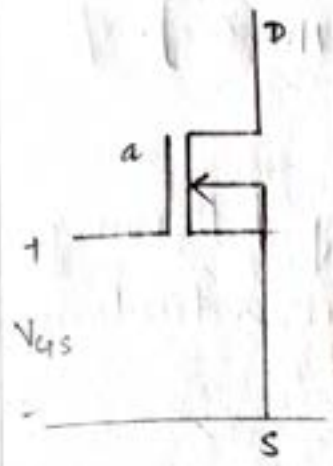
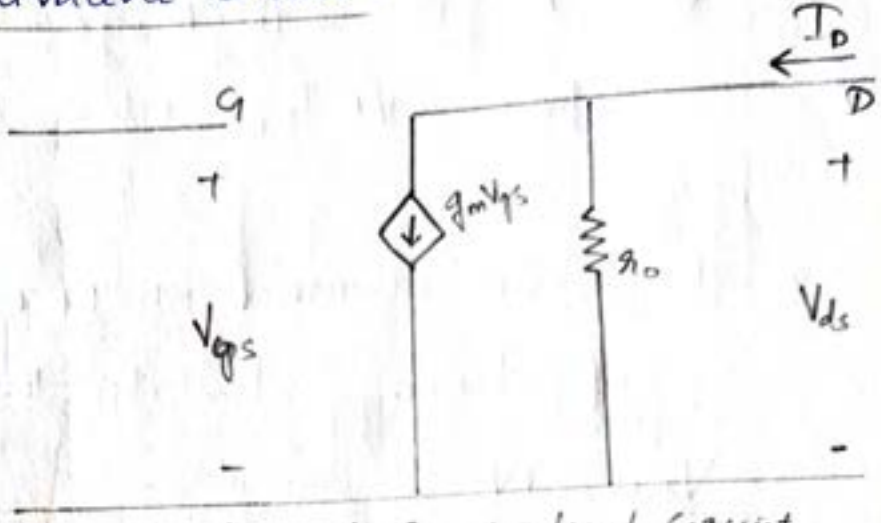
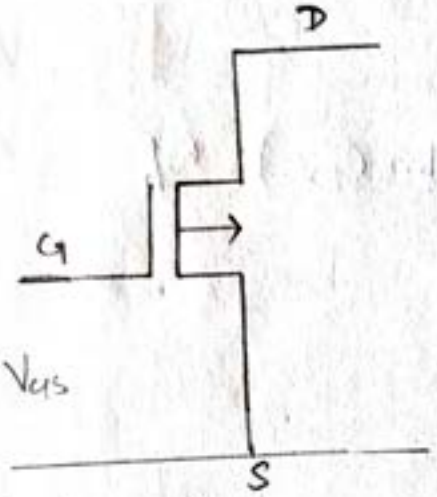
Small Signal Equivalent Circuit.



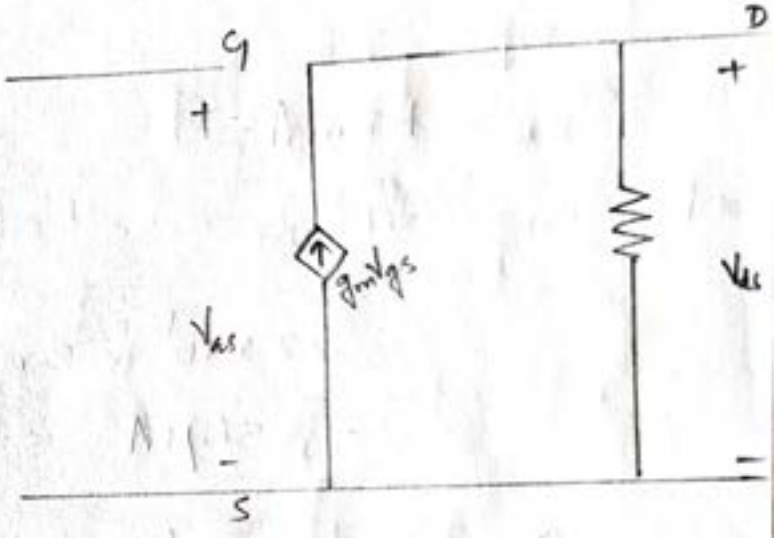
N-channel MOSFET



Small Signal Equivalent Circuit



P-channel MOSFET



Small Signal Equivalent circuit.

Because of the presence of SiO_2 layer, the gate terminal is isolated from the main structure of the device. Therefore, the i/p resistance of the MOSFET is extremely large which is represented by an open circuit. MOSFET act as a voltage controlled current source which is shown in the o/p side as $g_m V_{gs}$. The finite output resistance $r_o = \frac{1}{\lambda . I_{DQ}}$

$$r_o = \frac{1}{\lambda [K (V_{GS} - V_{TH})^2]}$$

where λ is the channel length modulation parameter.

The transconductance,

$$g_m = 2\sqrt{K I_{DQ}} \quad \text{where} \quad K = \left(\tfrac{1}{2}\mu_n C_{ox}\right) \cdot W/L$$

Q for an n-channel MOSFET having following specifications, calculate the transconductance.

$V_{TH} = 1V$

$\frac{1}{2}\mu_n C_{ox} = 22\,\mu A/V^2$

$W/L = 38$

$I_{DQ} = 1.2\,mA$.

Sol: $g_m = 2\sqrt{K I_{DQ}}$; $K = (\frac{1}{2}\mu_n C_{ox}) \cdot W/L$

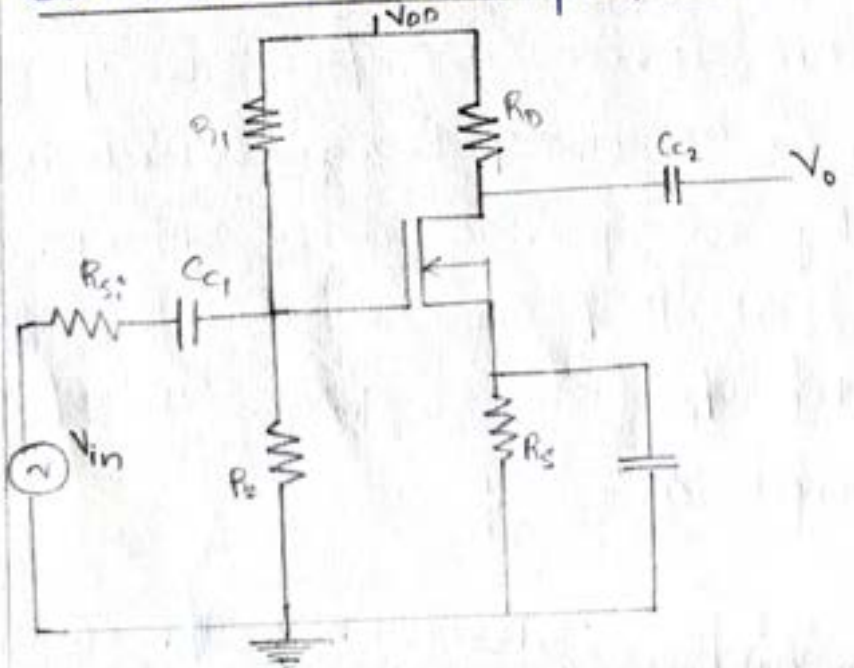
$= 22 \times 10^{-6} \times 38$

$= 836\,\mu A$.

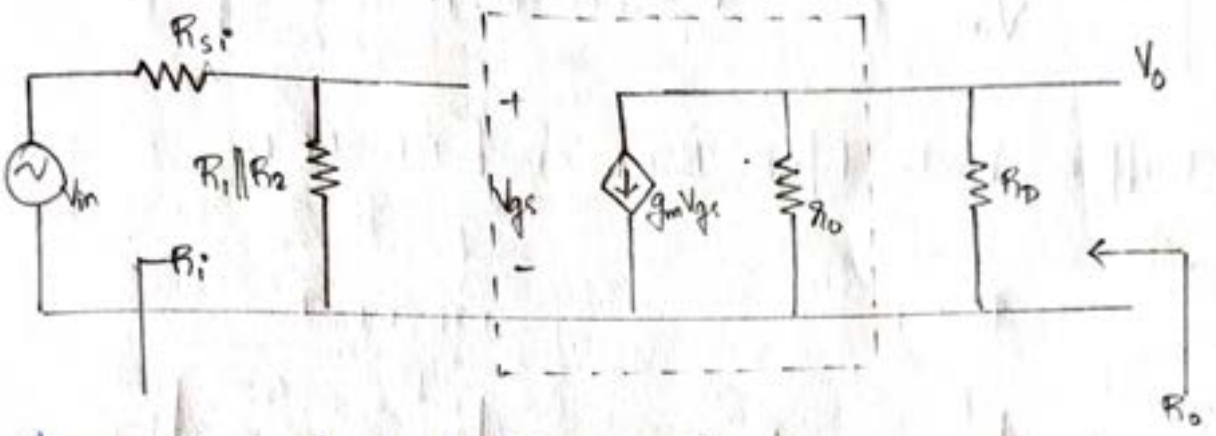
$$g_m = 2\sqrt{836\times10^{-6} \times 1.2\times10^{-3}}$$

$$g_m = 2\,mA/V$$

Common Source Amplifier:



Here the biasing circuit used is a voltage divider. R_1 and R_2 make a biasing circuit which biase a MOSFET in its Saturation region. Source resistance [Rsi] is very small.

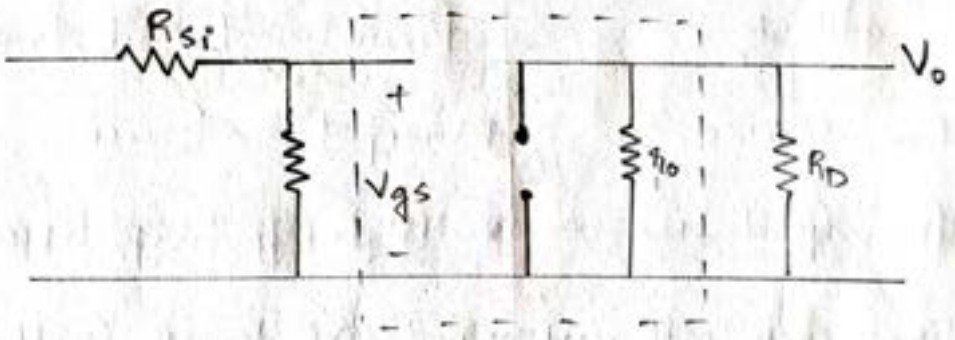


Input impedance = $R_i = R_1 \| R_2$

Output impedance $R_o = r_o \| R_D$

In order to find R_o we can Set $V_{in} = 0$

$\therefore V_{gs} = 0$ and $g_m V_{gs} = 0$ ie; open circuit.



Output impedance $R_o = r_o \| R_D$

Voltage Gain:

$$A_V = \frac{V_o}{V_{in}}$$

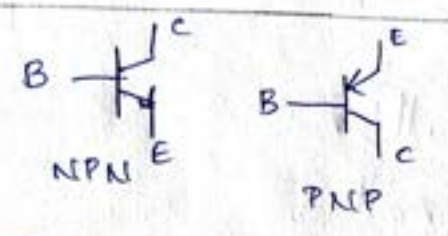
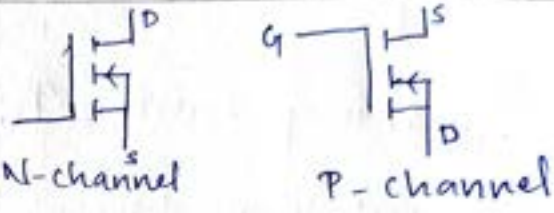
$$V_o = -g_m V_{gs} (r_o \| R_D)$$

$$V_{gs} = V_{in} \frac{(R_1 \| R_2)}{R_{si} + (R_1 \| R_2)}$$

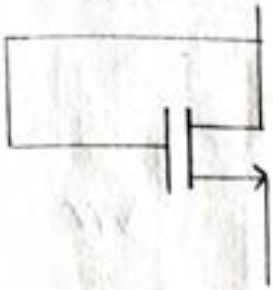
$$V_o = -g_m \left[V_{in} \frac{(R_1 \| R_2)}{R_{si} + (R_1 \| R_2)} \right] \times r_o \| R_D$$

$$A_v = \frac{V_o}{V_{in}} = -g_m \left[\frac{R_1 \| R_2}{R_{si} + (R_1 \| R_2)} \right] r_o \| R_D$$

Q Differentiate b/w BJT and MOSFET.

BJT	MOSFET
	
* BJT is a 3 terminal SC used for switching and amplifications of signals.	* MOSFET is a 4 teminal SC device which is used for switching amplification.
* Three terminals: base, emitter, collector	* 4 terminals are gate, source, drain and substrate.
* Bipolar device	* Unipolar device
* low i/p impedance	* High i/p impedence.
* Negative temp coefficient	* positive temp coefficient
* Consumes more power than MOSFET	* Power consumed is less than BJT
* Preffered for low current application. It is used as amplifier, oscillators and electronic switches.	* Suitable for high current application. It is also used in power supplies etc.

Common Source Stage With Diode Connected Load.

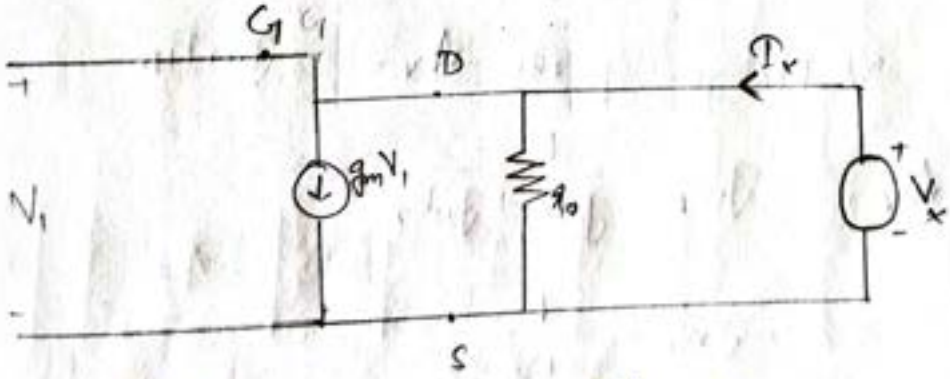


Diode Connected n-Channel MOSFET

Diode connected P-channel MOSFET

In many CMOS technologies, it is difficult to fabricate resistor. So it is desirable to replace R_D [drain resistance]

A MOSFET can operate as a small signal resistor if its gate and drain are shorted. Then it is called diode connected device.



$$R_x = \frac{V_x}{I_x} \qquad I_x = \frac{V_x}{r_o} + g_m V_1$$

$V_1 = V_x$ [∵ they both come parallel & no V_{gs} loop b/w them]

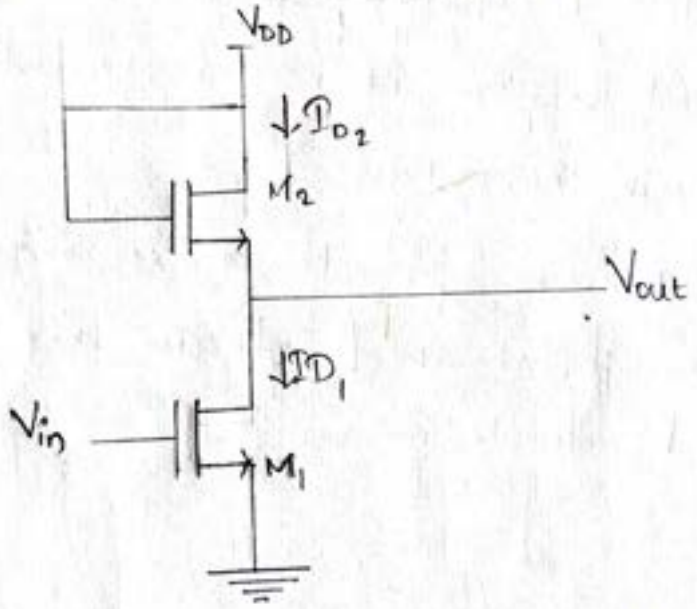
$$I_x = \frac{V_x}{r_o} + g_m V_x$$

$$I_x = V_x \left[\frac{1}{r_o} + g_m\right]$$

$$Z_x = \frac{V_x}{I_x}$$

$$\therefore Z_x = \frac{1}{\frac{1}{r_o} + g_m} \simeq \frac{1}{g_m}$$

If we consider the body effect, then the impedance, $\boxed{Z_x = \frac{1}{g_m + g_{mb}}}$



$$A_v = -g_m R_D$$

$$R_D = Z_x = \frac{1}{g_m + g_{mb}}$$

Here, the Voltage gain $A_v = -g_m R_D$

$$A_v = -g_{m_1} \cdot \frac{1}{g_{m_2} + g_{mb_2}}$$

$$= -\frac{g_{m_1}}{g_{m_2}} \cdot \frac{1}{1 + \frac{g_{mb_2}}{g_{m_2}}}$$

$$\boxed{A_v = -\frac{g_{m_1}}{g_{m_2}} \cdot \frac{1}{1+\eta}} \quad ; \quad \eta = \frac{g_{mb_2}}{g_{m_2}} \quad \text{---} (1)$$

Transconductance in terms of device dimensions

$$g_m = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

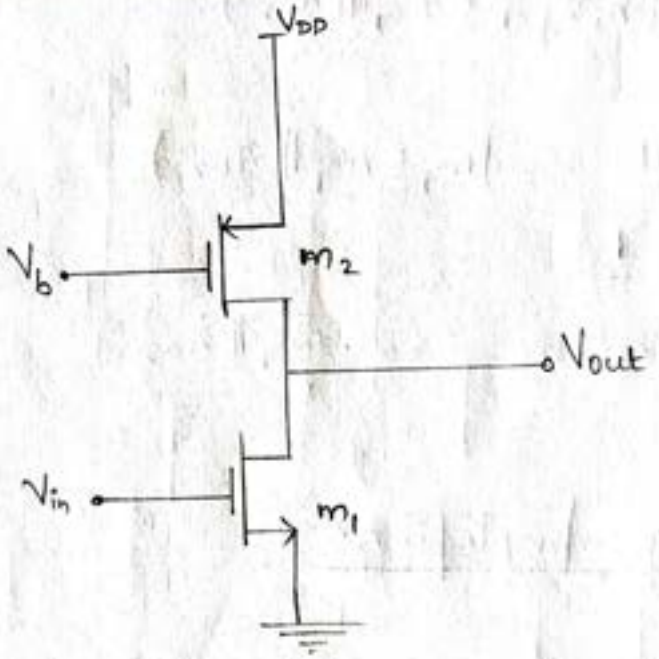
① $\Rightarrow A_V = -\dfrac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \cdot I_{D1}}}{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{D2}}} \cdot \dfrac{1}{1+\eta}$

$I_{D_1} = I_{D_2}$

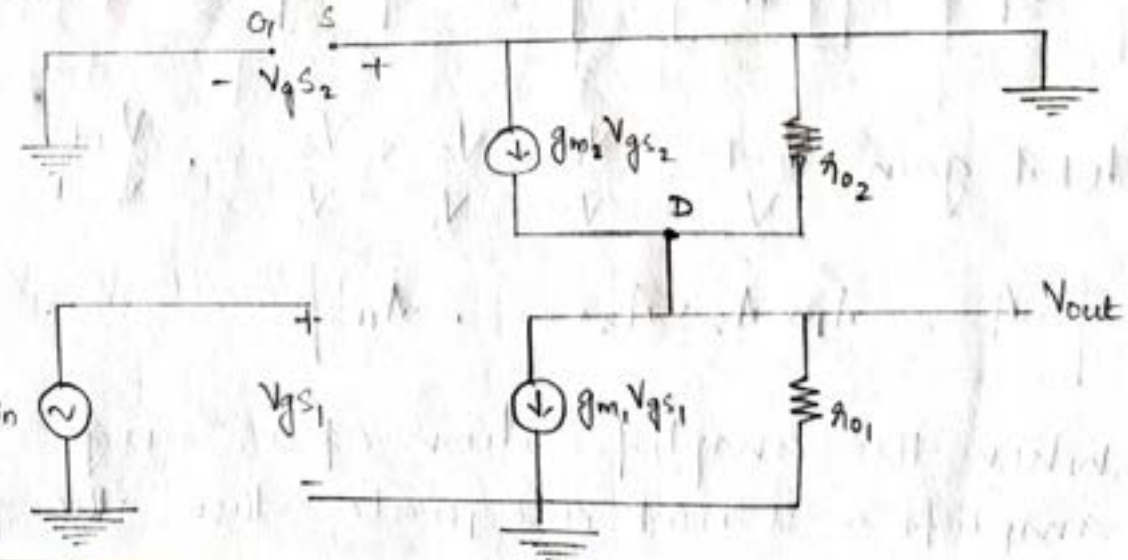
$$\boxed{A_V = -\frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}} \cdot \frac{1}{1+\eta}}$$

If we neglect the effect of η we can say, the gain is almost constant.

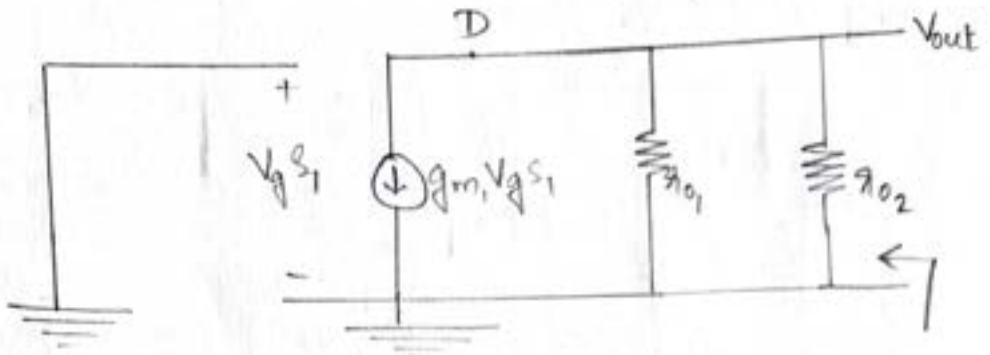
Common Source Stage With Current Source load.



Small Signal Equivalent Ckt :



The Small Signal equivalent can be redrawn as:



Here,

Voltage gain; $A_v = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{gs_1}}$

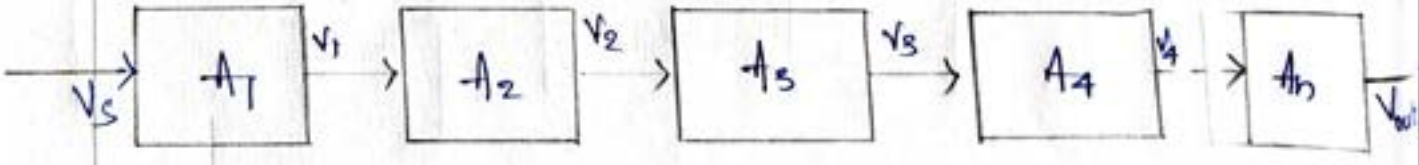
$V_{out} = -g_{m_1} V_{gs_1} (r_{o_1} \| r_{o_2})$

$\therefore \boxed{A_v = \frac{V_{out}}{V_{gs_1}} = -g_{m_1} (r_{o_1} \| r_{o_2})}$

Output Impedance, $r_o = (r_{o_1} \| r_{o_2})$

18/4/23

Multi-Stage Amplifiers:



Total gain, $\frac{V_{out}}{V_s} = \frac{V_1}{V_s} \times \frac{V_2}{V_1} \times \frac{V_3}{V_2} \cdots \frac{V_{out}}{V_{n-1}}$

$$\boxed{A = A_1 \times A_2 \times A_3 \times \cdots A_N}$$

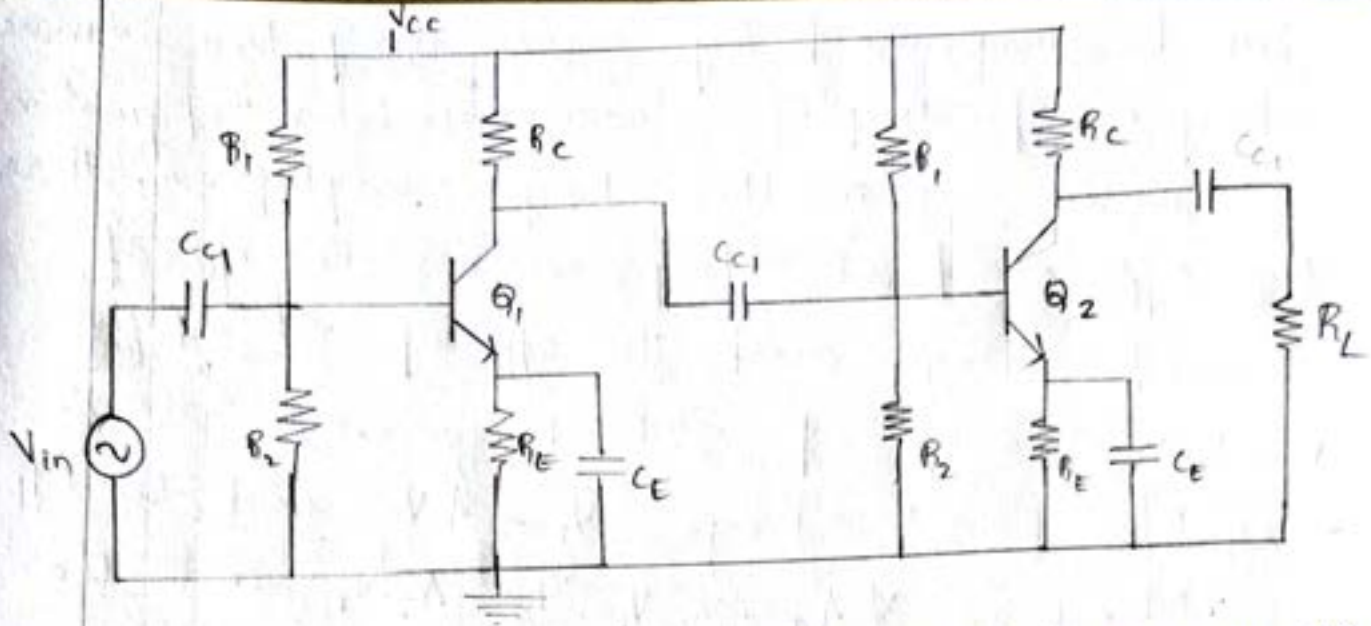
When the amplification of a single stage amplifier is not adequate, then the gain

can be improved by cascading two or more stages of amplification. Such a configuration is known as multi-stage amplifier. Here the o/p of first stage makes the i/p of second stage and the o/p of 2nd stage makes the i/p of 3rd stage and so on. The o/p of 1st stage $V_1 = A_1 V_s$ and the o/p of 2nd stage ~~$A_2 = V_2 \cdot V_1$~~ $V_2 = A_2 \cdot V_1$ and the overall gain:

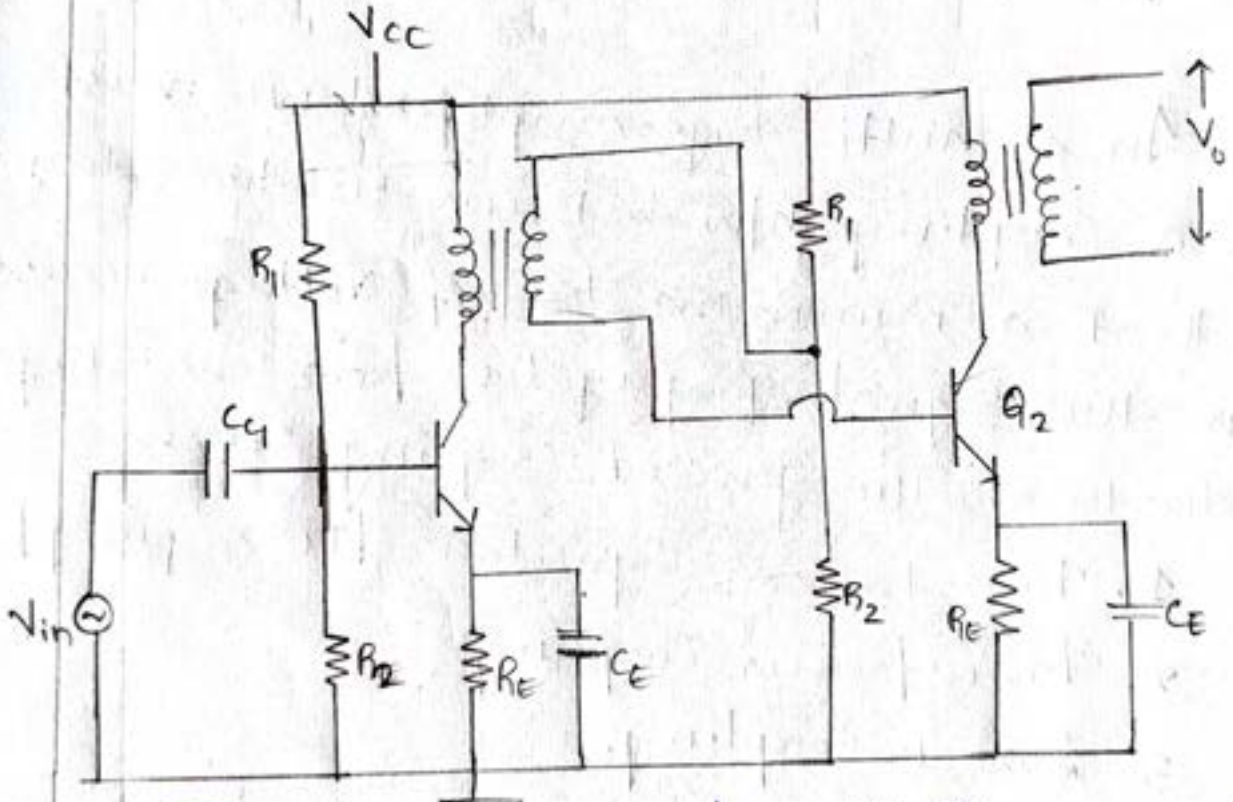
$$\frac{V_{out}}{V_s} = \frac{V_1}{V_s} \times \frac{V_2}{V_1} \times \frac{V_3}{V_2} \cdots \frac{V_{out}}{V_{n-1}}$$

In a multi stage amplifier, we must use a coupling n/w between the two stages so that a minimum loss of voltage occurs when the signal propagates from one stage to another. The general coupling schemes are 1. Resistance - Capacitance [RC coupling]

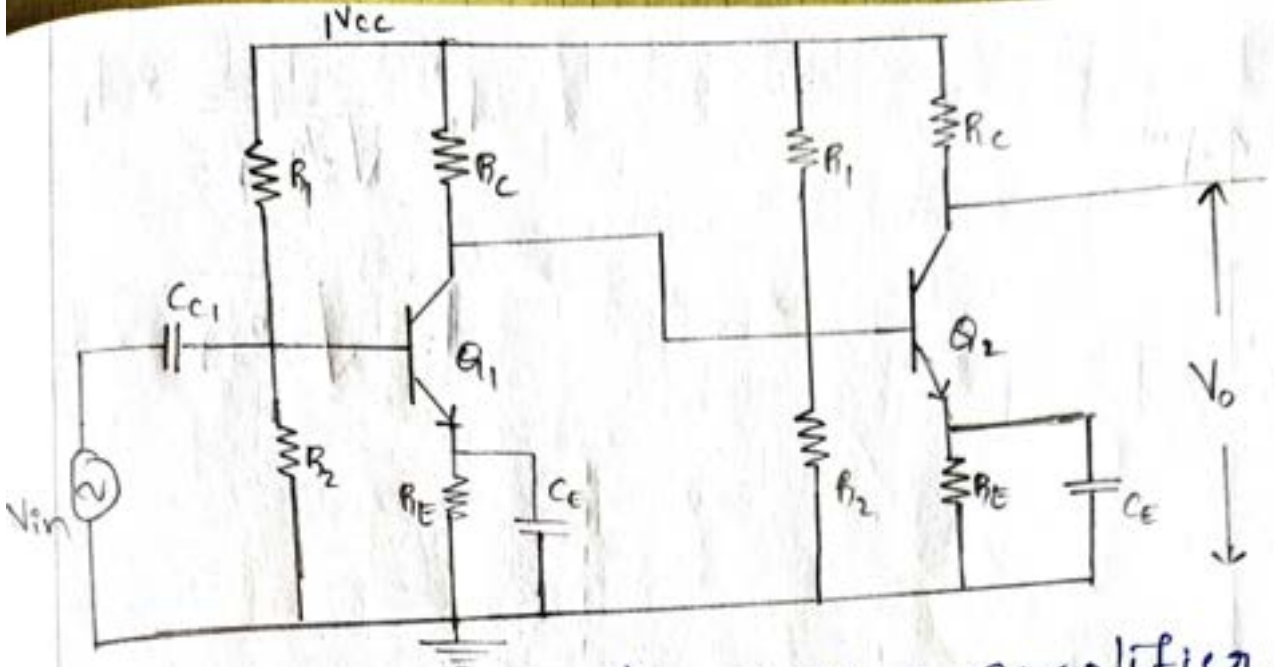
2. Transformer Coupling
3. Direct Coupling.



RC coupled Amplifier [Multi-stage amplifier]



Transformer coupled multi Stage amplifier.



Direct coupled Multistage amplifier.

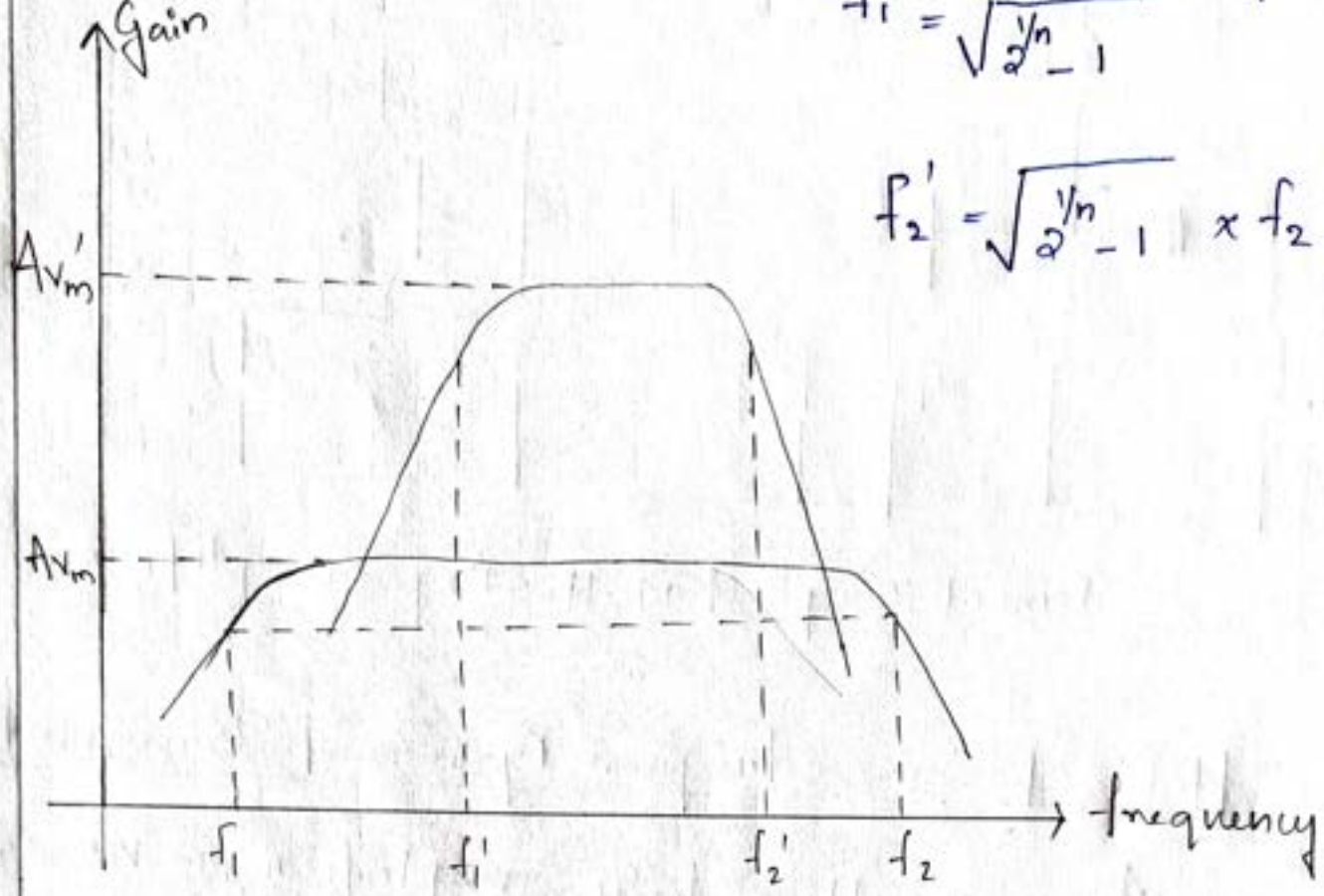
Effect of Cascading on Gain and Bandwidth.

In a multi-stage amplifier, a no. of stages are cascaded to obtain higher values of voltage gain. If n no. of stages are cascaded and A_{Vm} is the mid band gain of individual stage, then the overall gain becomes; $A_V = [A_{Vm}]^n$

But the bandwidth of amplifier does not remain the same. It will decrease with cascading. ie; the upper cut off frequencies and the lower cut off frequency increases It happens because greater no. of stages means more no. of capacitors. and each capacitor affects the frequency response adversly.

$$f_1' = \frac{1}{\sqrt{2^{1/n} - 1}} \times f_1$$

$$f_2' = \sqrt{2^{1/n} - 1} \times f_2$$

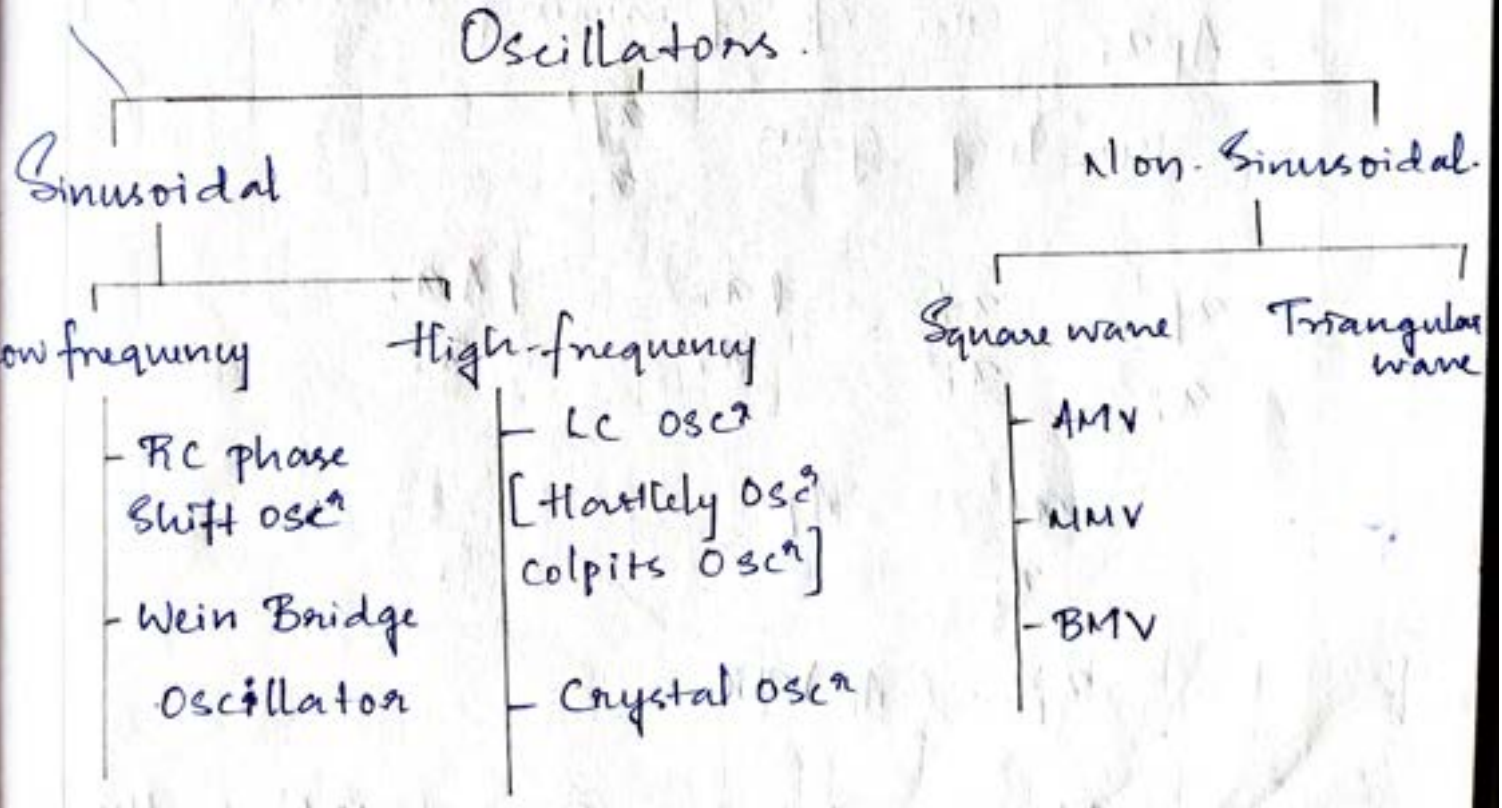


MODULE - IV

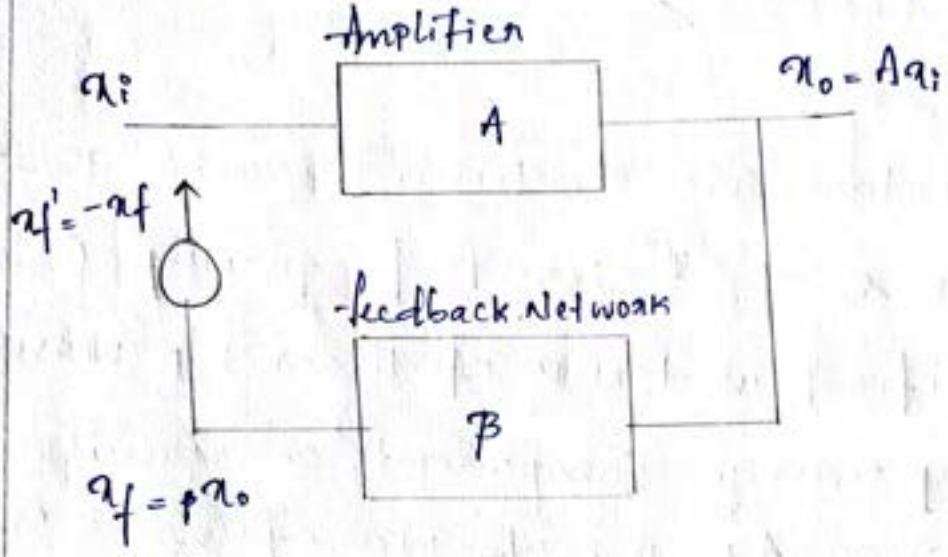
OSCILLATORS

Oscillators

Oscillators are electronic circuits that generate wave forms of desired frequency. Oscillators are classified in terms of their o/p waveform, frequency range, components or circuit configuration. If the o/p waveform is sinusoidal then it is called sinusoidal oscillators otherwise called relaxation oscillators [Square, triangular or Sawtooth waveforms]



Principle of Oscillators / criteria for Oscillation



In figure, amplifier provides an o/p signal $x_o = Ax_i$. Here the feedback signal $x_f = \beta x_o$ $= A\beta x_i$. The o/p of mixing circuit $= -x_f$

So the loop gain $= \frac{x_f'}{x_i}$

$$\frac{x_f'}{x_i} = \frac{-x_f}{x_i} = \frac{-\beta x_o}{x_i} = \frac{-\beta A x_i}{x_i}$$

$$\frac{x_f'}{x_i} = -A\beta$$

$$x_f' = (-A\beta)x_i$$

If $x_f' = x_i$, we can connect x_f' as the i/p of the circuit instead of x_i. for that the condition to be satisfied is

$-A\beta = 1$ i.e.

$$\left.\begin{array}{l} \angle A\beta = 0, 360^\circ \\ |A\beta| = 1 \end{array}\right\}$$ Barkhausen's criteria

Wein Bridge ~~Criteria~~ Oscillator.

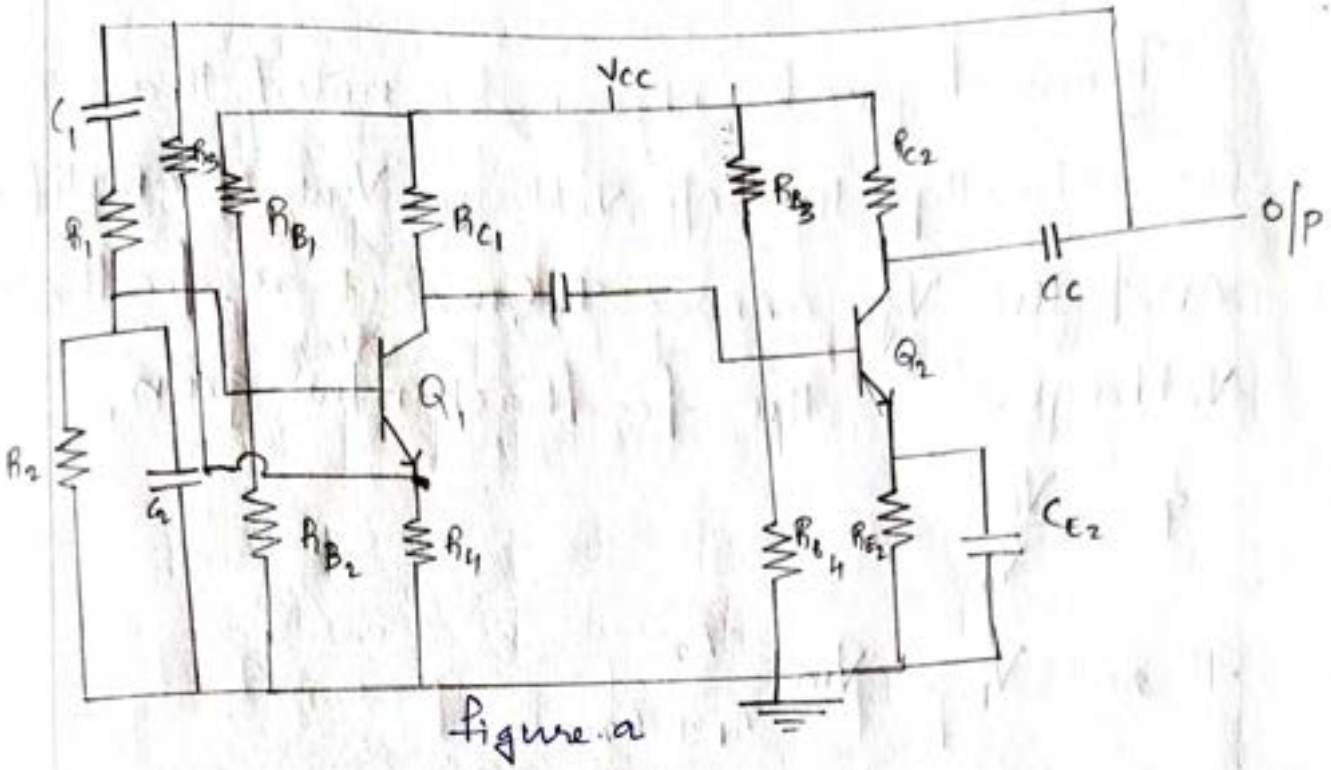


figure. a

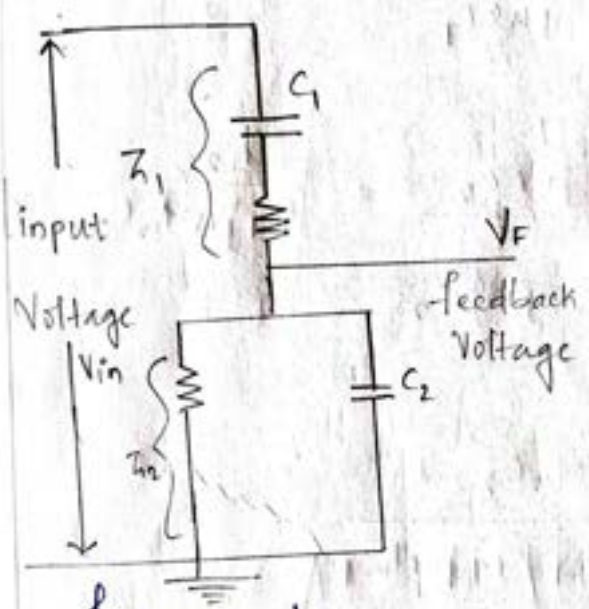


figure. b

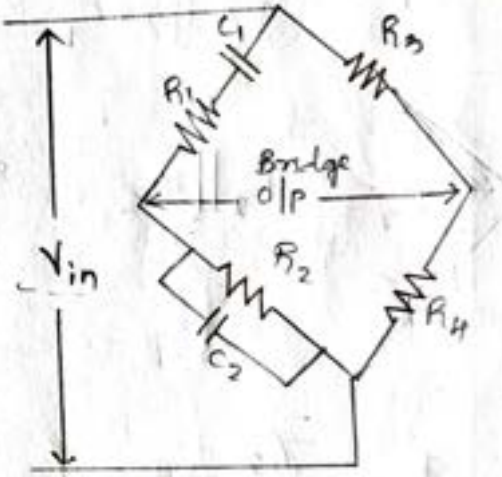


figure. c

Wein bridge oscillator uses wein bridge as a feedback network. It has two frequency Sensitive arm [R_1C_1 in series and R_2C_2 in Parallel] which decides the oscillator frequency.

It has two feedback networks, positive feedback generates ~~gives~~ oscillation and negative feedback gives stability.

27/4/23 Analysis

From figure b, it can be noted that V_{in} is actually the o/p voltage V_{out} of amplifier and the V_{ge} across R_2C_2 act as feedback voltage. So the feedback voltage gain,

$$\beta = \frac{V_F}{V_{in}}$$

Here, $V_F = V_{in} \frac{Z_2}{Z_1 + Z_2}$

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$

$$Z_2 = R_2 \| C_2 = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}} = \frac{R_2}{1 + j\omega R_2 C_2}$$

$$\beta = \frac{Z_2}{Z_1 + Z_2} = \frac{\frac{R_2}{1 + j\omega R_2 C_2}}{\frac{R_2}{1 + j\omega R_2 C_2} + \left(\frac{1 + j\omega R_1 C_1}{j\omega C_1}\right)}$$

Substitute $j\omega = s$

$$\therefore \beta = \frac{\frac{R_2}{1 + sR_2C_2}}{\frac{R_2}{1 + sR_2C_2} + \left(\frac{1 + sR_1C_1}{sC_1}\right)}$$

$$= \frac{SR_2C_1}{SR_2C_1 + (1+SR_1C_1)(1+SR_2C_2)}$$

$$\beta = \frac{SR_2C_1}{SR_2C_1 + 1 + SR_2C_2 + SR_1C_1 + S^2R_2C_2R_1C_1}$$

$$\beta = \frac{SR_2C_1}{S^2(R_1C_1R_2C_2) + S[R_1C_1 + R_2C_2 + R_2C_1] + 1}$$

Substitute $S = j\omega$.

$\therefore S^2 = -\omega^2$

$$\beta = \frac{j\omega R_2C_1}{1 - \omega^2(R_1C_1R_2C_2) + j\omega[R_1C_1 + R_2C_2 + R_2C_1]}$$

Multiplying with complex conjugate of denominator on numerator and denominator.

$$\beta = \frac{j\omega R_2C_1\left[1 - \omega^2(R_1C_1R_2C_2) - j\omega[R_1C_1 + R_2C_2 + R_2C_1]\right]}{\left[1 - \omega^2(R_1C_1R_2C_2)\right]^2 + \omega^2[R_1C_1 + R_2C_2 + R_2C_1]^2} \quad \text{---(1)}$$

Equate the imaginary part equal to zero.

$$j\omega R_2C_1\left[1 - \omega^2R_1C_1R_2C_2\right] = 0$$

$$1 - \omega^2R_1C_1R_2C_2 = 0$$

$$\omega^2R_1C_1R_2C_2 = 1 \quad ; \quad \omega^2R^2C^2 = 1 \quad \left[\text{If } \begin{matrix} R_1 = R_2 = R \\ C_1 = C_2 = C \end{matrix}\right]$$

$$\omega^2 = \frac{1}{R_1C_1R_2C_2}$$

$$\left(\frac{1}{2\pi f}\right)^2 = \frac{1}{R_1 C_1 R_2 C_2} = (2\pi f)^2$$

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then,

$$f = \frac{1}{2\pi RC}$$

Frequency of Oscillation of Wein Bridge Oscillator

$$f = \frac{1}{2\pi RC}.$$

So β from equation ①;

$$\beta = \frac{j\omega R_2 C_1 (1 - \omega R_1 C_1 R_2 C_2) + \omega^2 R_2 C_1 (R_1 C_1 + R_2 C_2 + R_2 C_1)}{[1 - \omega^2 (R_1 C_1 R_2 C_2)]^2 + \omega^2 (R_1 C_1 + R_2 C_2 + R_2 C_1)^2}$$

$$\beta = \frac{j\omega RC (1 - \omega^2 R^2 C^2) + \omega^2 RC \cdot 3RC}{[1 - \omega^2 R^2 C^2]^2 + \omega^2 (3RC)^2}$$

Then equate the real part on both sides,

$$\beta = \frac{\omega^2 R^2 C^2 \cdot 3}{1 - \omega^2 R^2 C^2 + \omega^2 (3RC)^2} \quad \because \omega^2 R^2 C^2 = 1$$

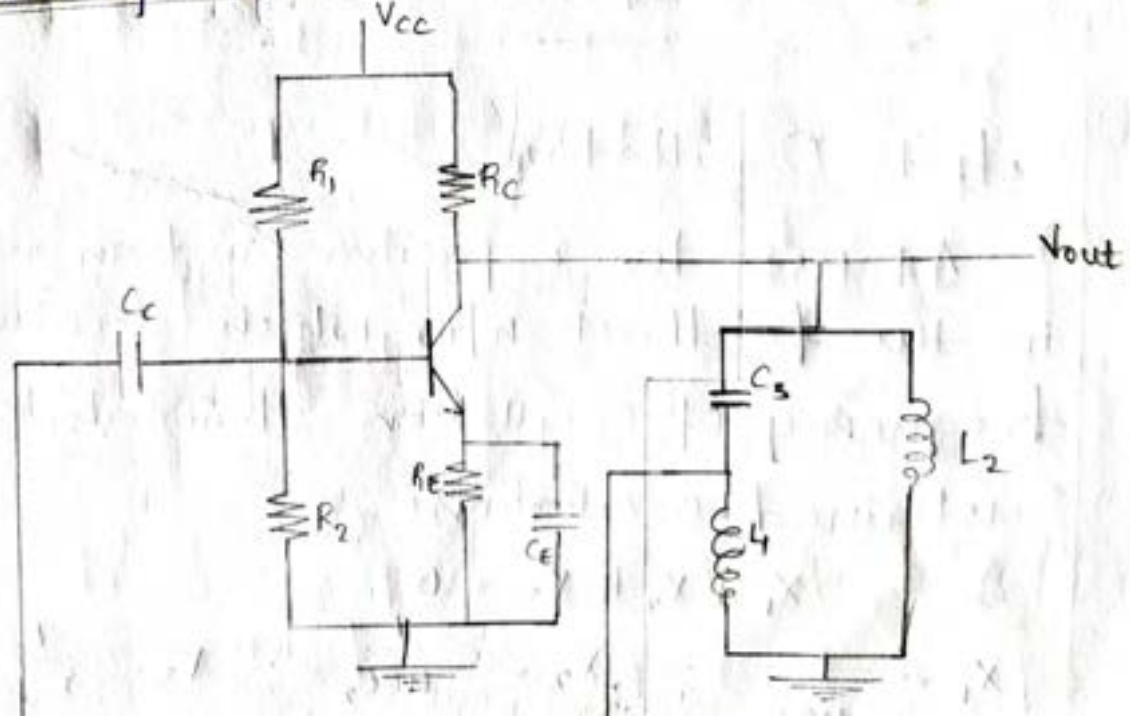
$$\beta = \frac{3}{9} = \frac{1}{3}$$

So for sustained oscillation magnitude of $A\beta = 1$. Since $\beta = \frac{1}{3}$; $A = 3$

Amplitude Stabilisation.

For sustained oscillations in a wein bridge oscillator, the gain of amplifier should be greater than or equal to 3. But this gain should not be too large as it will distort the o/p waveform. Therefore, the amplifier gain should be controlled. This is achieved by introducing a negative feedback by keeping the resistor R_4 in the emitter of Q_1 unbypassed. This introduce a current series feedback and the process of gain reduction using negative feedback is known as amplitude stabilisation.

Hartley Oscillator.



Hartley Oscillator is a high frequency LC oscillator which uses two inductors and a capacitor in the feedback n/w which decides the frequency of oscillation. For sustained oscillation, the condition to be satisfied is $X_1 + X_2 + X_3 = 0$.

Here, $X_1 = \omega L_1$; $X_2 = \omega L_2$; $X_3 = \frac{-1}{\omega C_3}$

$$X_1 + X_2 + X_3 = 0$$

$$\omega L_1 + \omega L_2 - \frac{1}{\omega C_3} = 0$$

$$\omega (L_1 + L_2) = \frac{1}{\omega C_3} \Rightarrow \omega^2 = \frac{1}{C_3 (L_1 + L_2)}$$

$$2\pi f = \omega = \frac{1}{\sqrt{C_3 (L_1 + L_2)}}$$

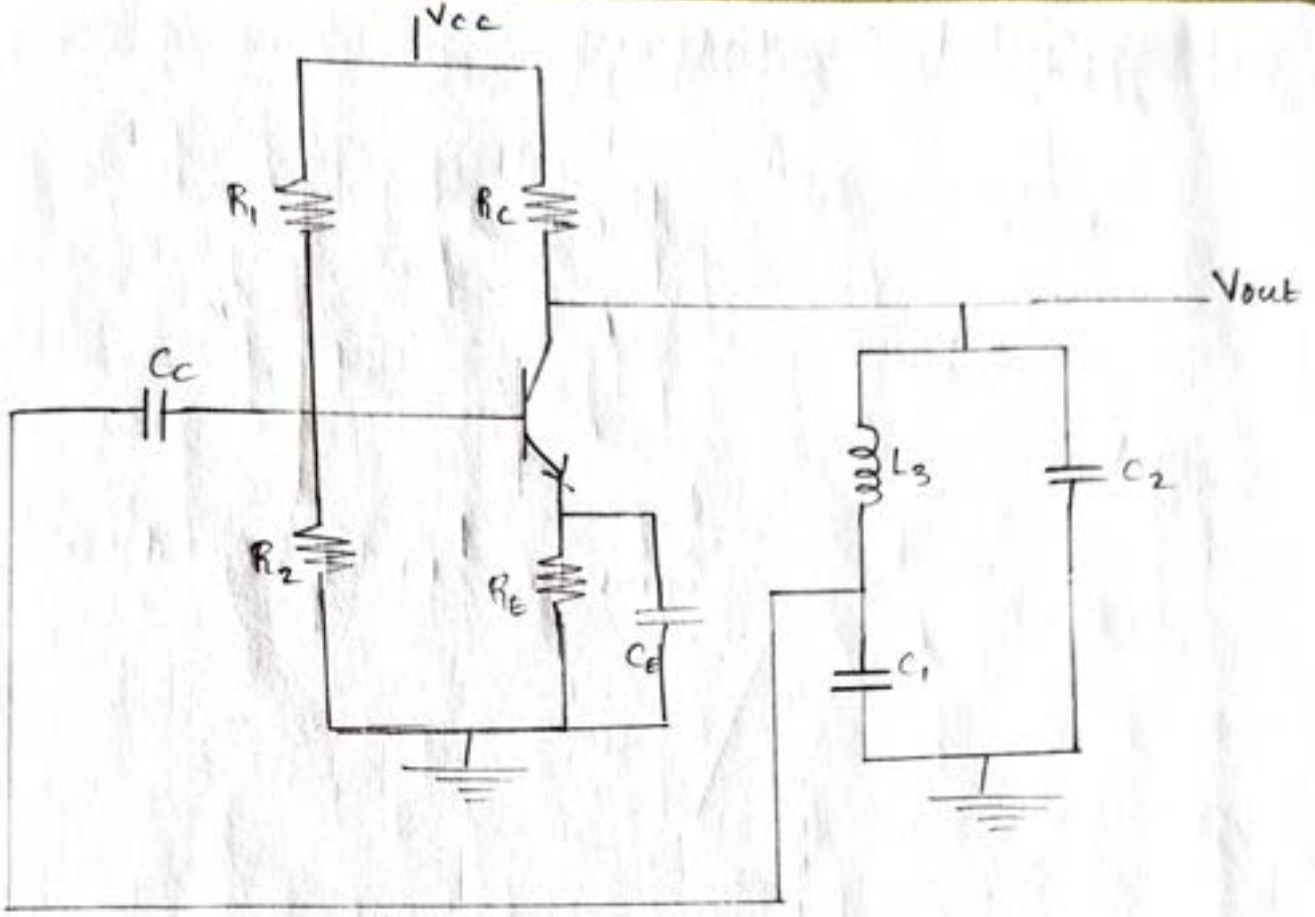
$$f = \frac{1}{2\pi \sqrt{C_3 (L_1 + L_2)}}$$

Colpits Oscillator.

It uses two capacitors and an inductor in the feedback n/w which decides the frequency of oscillation. Here also for sustained oscillations

$$X_1 + X_2 + X_3 = 0$$

$X_1 = \frac{-1}{\omega C_1}$; $X_2 = \frac{-1}{\omega C_2}$; $X_3 = \omega L_3$



$$X_1 + X_2 + X_3 = 0$$

$$-\frac{1}{\omega C_1} - \frac{1}{\omega C_2} + \omega L_3 = 0$$

$$\frac{1}{\omega C_1} + \frac{1}{\omega C_2} = \omega L_3 \Rightarrow \frac{1}{L_3(C_1+C_2)} = \omega^2$$

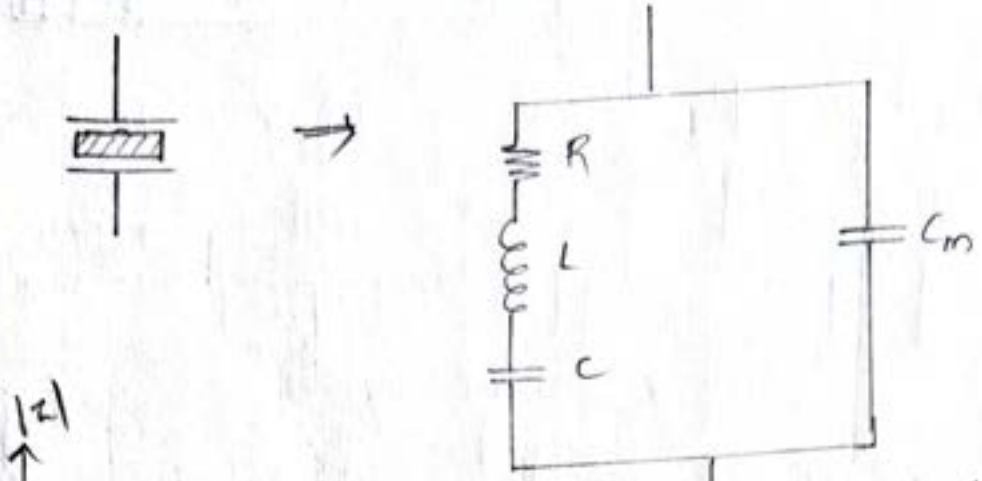
$$2\pi f = \omega = \frac{1}{\sqrt{L_3(C_1+C_2)}} \Rightarrow f = \frac{1}{2\pi\sqrt{L_3(C_1+C_2)}}$$

$$\frac{1}{C_1} + \frac{1}{C_2} = \omega^2 L_3 \Rightarrow \frac{C_1+C_2}{C_1 C_2} = \omega^2 L_3$$

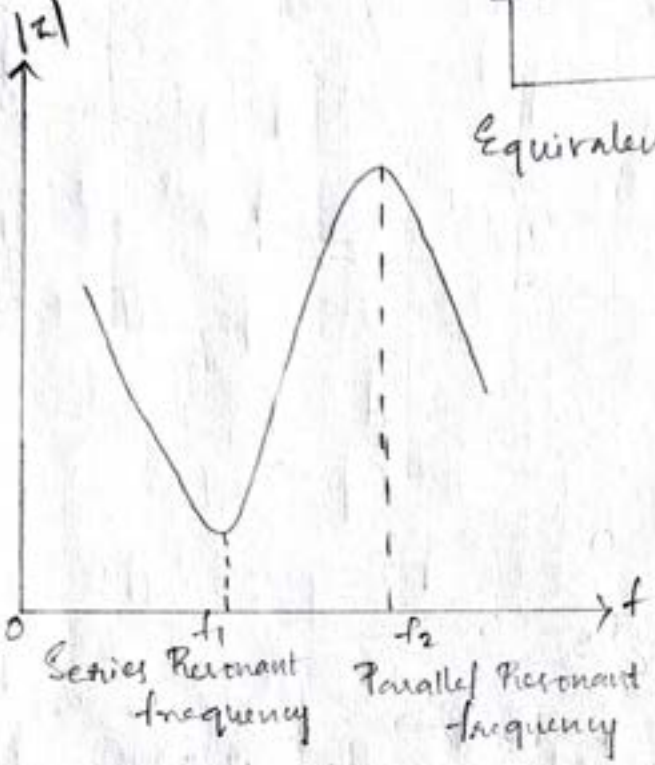
$$\omega^2 = \frac{1}{L_3}\left[\frac{C_1+C_2}{C_1 C_2}\right] \Rightarrow 2\pi f = \omega = \frac{1}{\sqrt{L_3\left(\frac{C_1 C_2}{C_1+C_2}\right)}}$$

$$f = \frac{1}{2\pi\sqrt{L_3\left[\frac{C_1 C_2}{C_1+C_2}\right]}}$$

Crystal Oscillator.



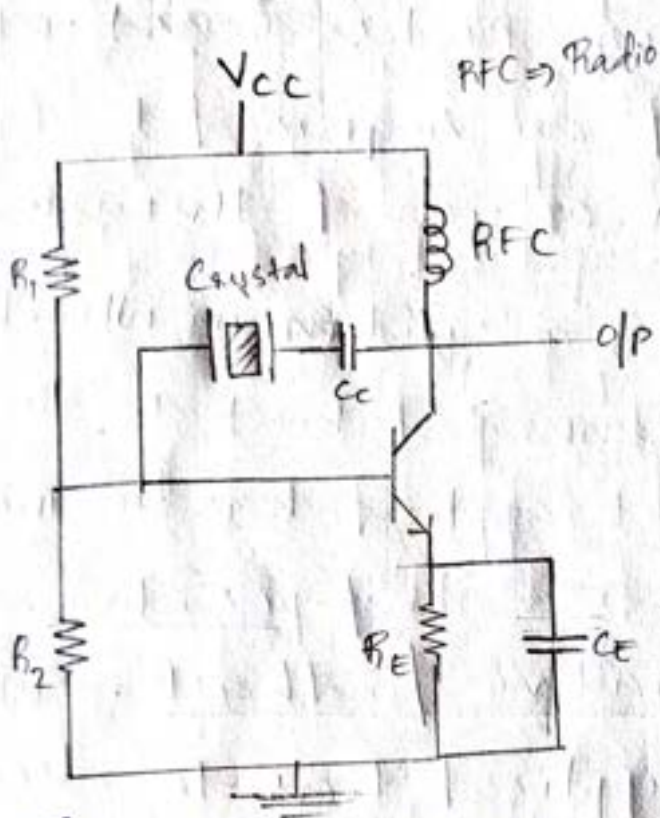
Equivalent ckt of Crystal Osc^n



A crystal oscillator is basically a tunned circuit oscillator using a piezo electric crystal as a resonant tank circuit. It has a greater stability in holding a constant frequency to which it is originally cut to operate. The main applications are in communication transmitors and recievers.

The crystal can have two resonant frequencies. One resonant condition occurs when the reactances of series RLC leg are equal and opposite. For this condition

the impedance is very low. The second resonance occurs at higher frequency and the reactance of series resonant leg equals reactance capacitor C_m. At this frequency crystal offers high impedance.



Series Resonant ckt.

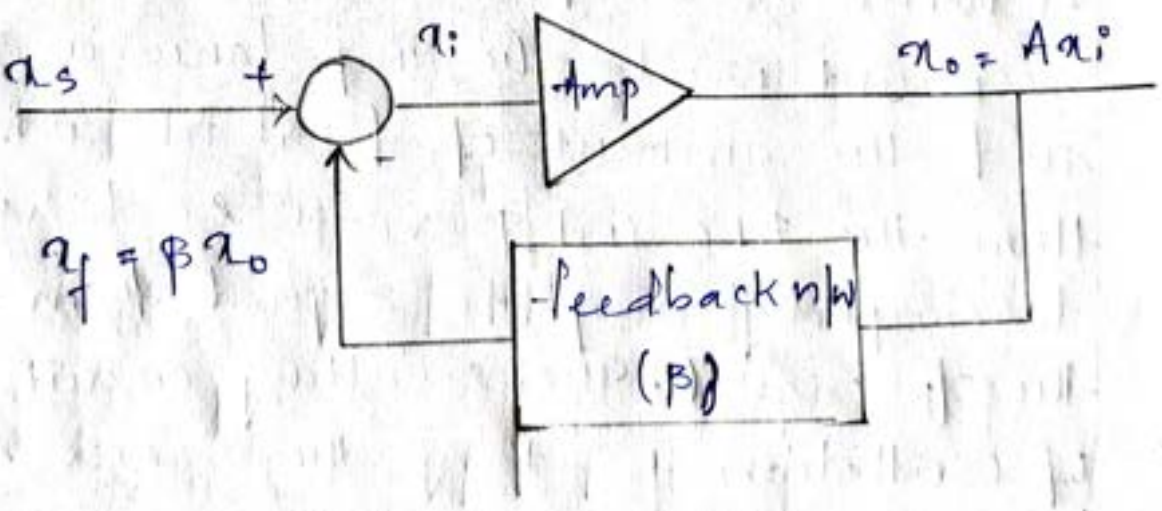
Here, the crystal is connected as a series element in the feedback path. At series resonant mode the impedance is smallest and the amount of feedback is maximum. Here the RLC coil provides DC bias by de-coupling any AC signal from affecting the O/P signal. The resulting circuits frequency of oscillation is set by the series resonant frequency of the crystal.

01/06/23

Feedback in Amplifiers.

The voltage gain, i/p and o/p impedance, bandwidth etc are few important characteristics of an amplifier. These parameters are more or less constant for an amplifier and are required to be controlled and is achieved through feedback.

The feedback is a system in which a portion of o/p is connected back to the i/p. When the feedback applied has to increase the i/p signal it is called positive or direct or regenerative feedback. When the feedback is applied has to decrease the i/p signal it is called negative or inverse or degenerative feedback.



A feedback amplifier essentially consist of two parts:

1. Amplifier
2. A feedback Stage.

The function of feedback n/w is to return a fraction of o/p energy (voltage/current) to the i/p of amplifier and the n/w is usually made up of resistors, capacitors & inductors.

Negative feedback	Positive feedback
$x_i = x_s - x_f$ $= x_s - \beta x_o$ $x_o = A x_i$ $x_o = A(x_s - \beta x_o)$ $= A x_s - A\beta x_o$ $x_o + A\beta x_o = A x_s$ $x_o[1 + A\beta] = A x_s$ $A_f = \frac{x_o}{x_s} = A_f = \frac{A}{1 + A\beta}$ Where A = gain without feedback A_f is the gain with feedback.	$x_i = x_s + x_f$ $= x_s + \beta x_o$ $x_o = A x_i$ $= A[x_s + \beta x_o]$ $= A x_s + A\beta x_o$ $x_o - A\beta x_o = A x_s$ $x_o[1 - A\beta] = A x_s$ $\frac{x_o}{x_s} = A_f = \frac{A}{1 - A\beta}$

Effect of Negative feedback on Amplifiers.

Eventhough the amplifier gain is reduced with negative feedback, the -ve feedback improves the performance of amplifier from so many other points of view. The major advantages of negative feedback are

1. It improves the stability of amplifier gain.
2. Reduces the distortion and noise.
3. Increases the i/p impedance.
4. Reduces the o/p impedance.
5. Increases the bandwidth.

Gain Stability:

A_f for negative feedback;

$$A_f = \frac{A}{1+A\beta} \qquad \because A\beta >> 1$$

$$A_f = \frac{A}{A\beta} = \frac{1}{\beta}$$

Since β is the feedback gain which depends only on passive component such as resistor whose values are fixed, the gain width feedback is almost stable.

9k/23

Feedback reduces distortion of noise

If A is the distortion without feedback and D_f the distortion with feedback then,

$$D_f = \frac{D}{1+A\beta}$$

Then the distortion is reduced by the same factor as the gain.

Feedback increases the input impedence

If Z_i = i/p impedence without feedback

Z_f = Z_i with feedback

$$Z_f = Z_i(1+A\beta)$$

If Z_o = o/p impedence without feedback

Z_{of} = o/p impedence with feedback

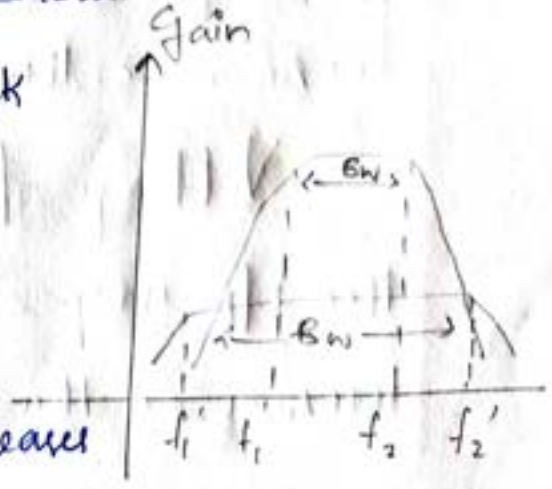
$$Z_{of} = \frac{Z_o}{1+A\beta}$$

Increase the Bandwidth.

B_w = Bandwidth without feedback

B_{wf} = " with feedback

$$B_{wof} = B_w(1+A\beta)$$



from the figure,

lower cut off frequency decreases from f_1 to f_1'. Then,

$$f_1' = \frac{f_1}{1+A\beta}$$

The upper cut off frequency increases from f_2 to f_2' then, $f_2' = f_2(1+A\beta)$

Feedback Topologies / connection Types.

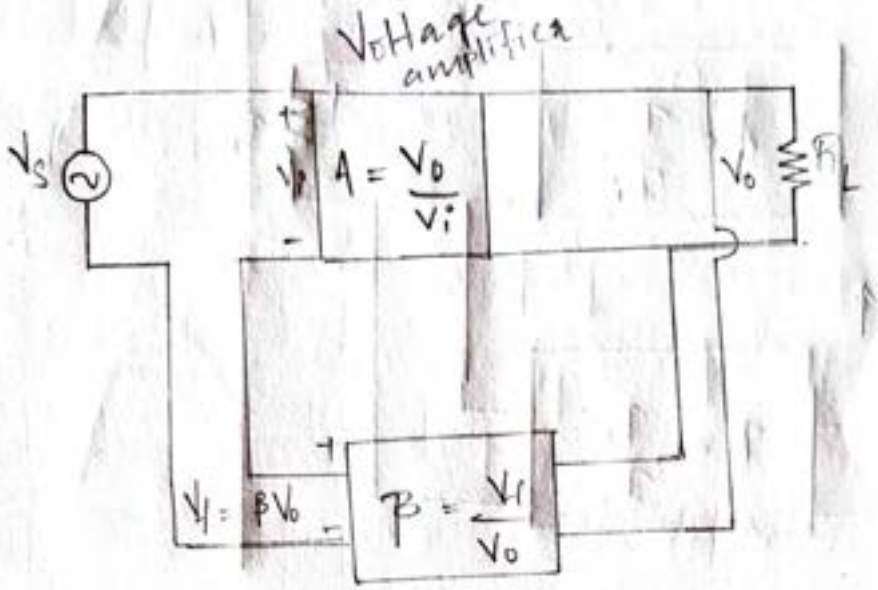
There are 4 basic ways of connecting the feedback signal. The voltage and current can be fed back either in series or parallel Specifically these can be

1. Voltage Series feedback
2. Voltage Shunt feedback
3. Current Series feedback
4. Current Shunt feedback

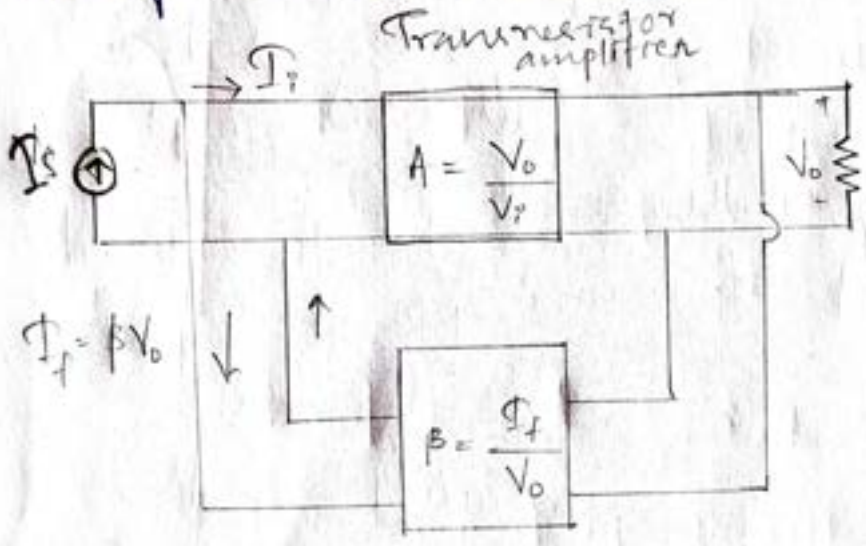
Series feedback connections increases the i/p impedence while Shunt feedback decreases the i/p impedence.

Voltage feedback tends to decrease the o/p impedence while current feedback increases the o/p impedence.

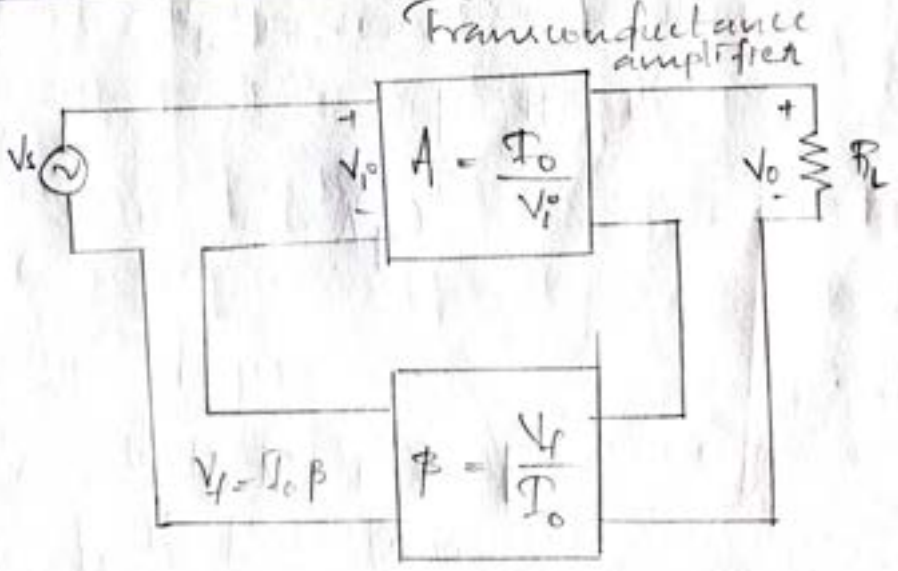
1. Voltage Series feedback.



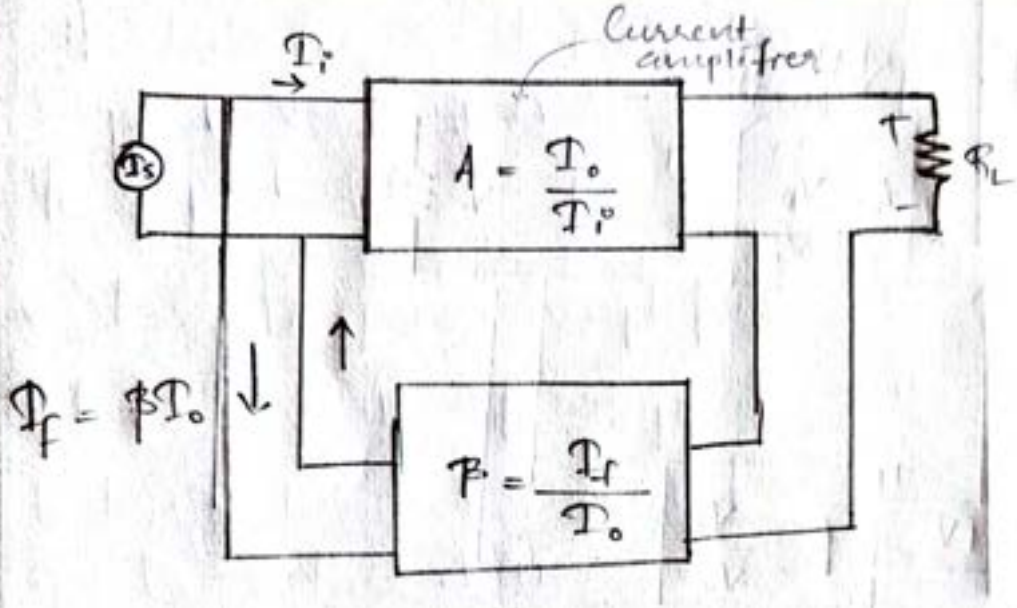
2. Voltage Shunt feedback.



3. Current Series feedback (Series-Series)



4. Current Shunt feedback (Series - Shunt)



5/6/23

V POWER AMPLIFIERS

A voltage amplifier provides voltage amplification primarily to increase the voltage of i/p signal. Large signal or power amplifier provide sufficient power to an output load.

Power amplifier is meant to raise the power level of i/p signal. Inorder to get large power at the o/p, it is necessary that the i/p signal voltage is large ie; why in an electronic system, a voltage amplifier always precedes the power amplifier and that is why power amplifier are called large signal amplifiers.

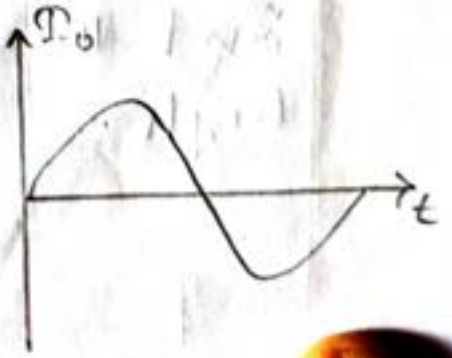
Power amplifier does not amplify power but it draws power from DC supply connected to the o/p circuit and converts it into useful ac signal power.

Thus power amplifier may be defined as a device that converts dc power to ac power whose action is controlled by input signal.

Classification of Power amplifier according to mode of operation.

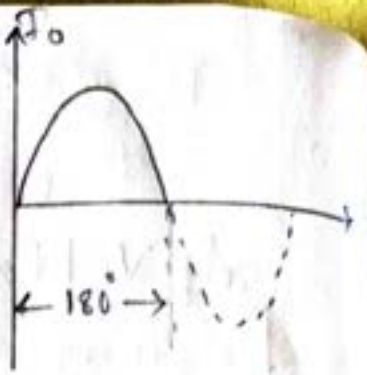
* Class A power amplifier

The o/p signal varies for full 360° of i/p signal.



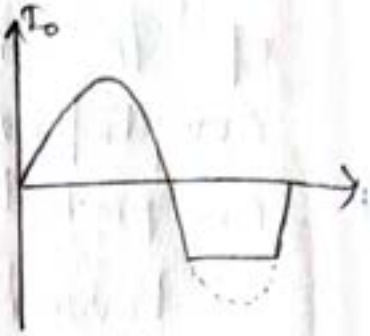
* Class B power amplifier

A class B circuit provides an o/p signal varying over one half of i/p signal cycle or for 180° of signal.



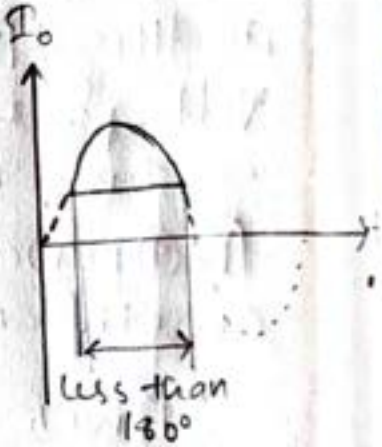
* Class AB power amplifier:

For class AB o/p signal occurs between 180° and 360° and is neither class A nor class B operation.



* Class C power amplifier:

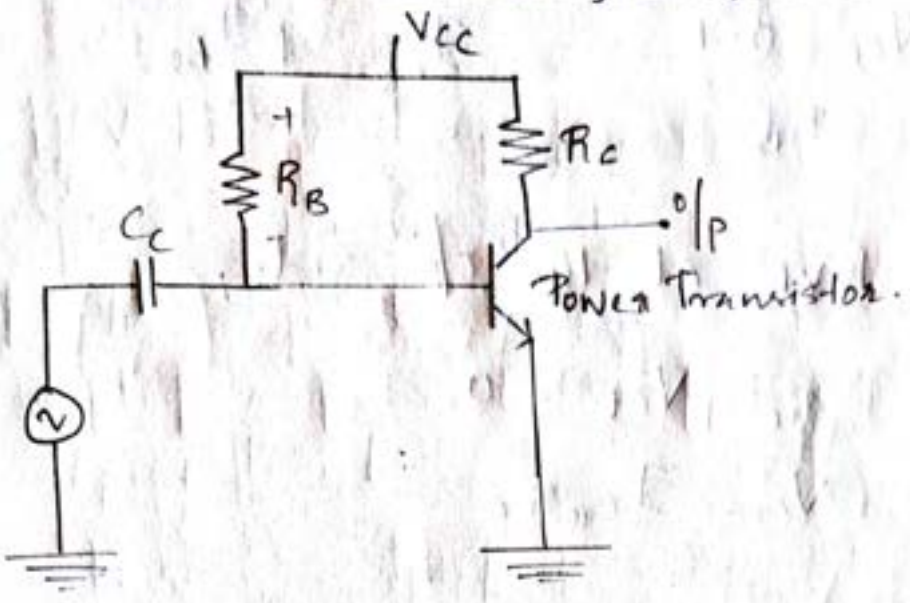
Here the transistor is so biased that o/p signal exist only for a period less than 180° of i/p signal.

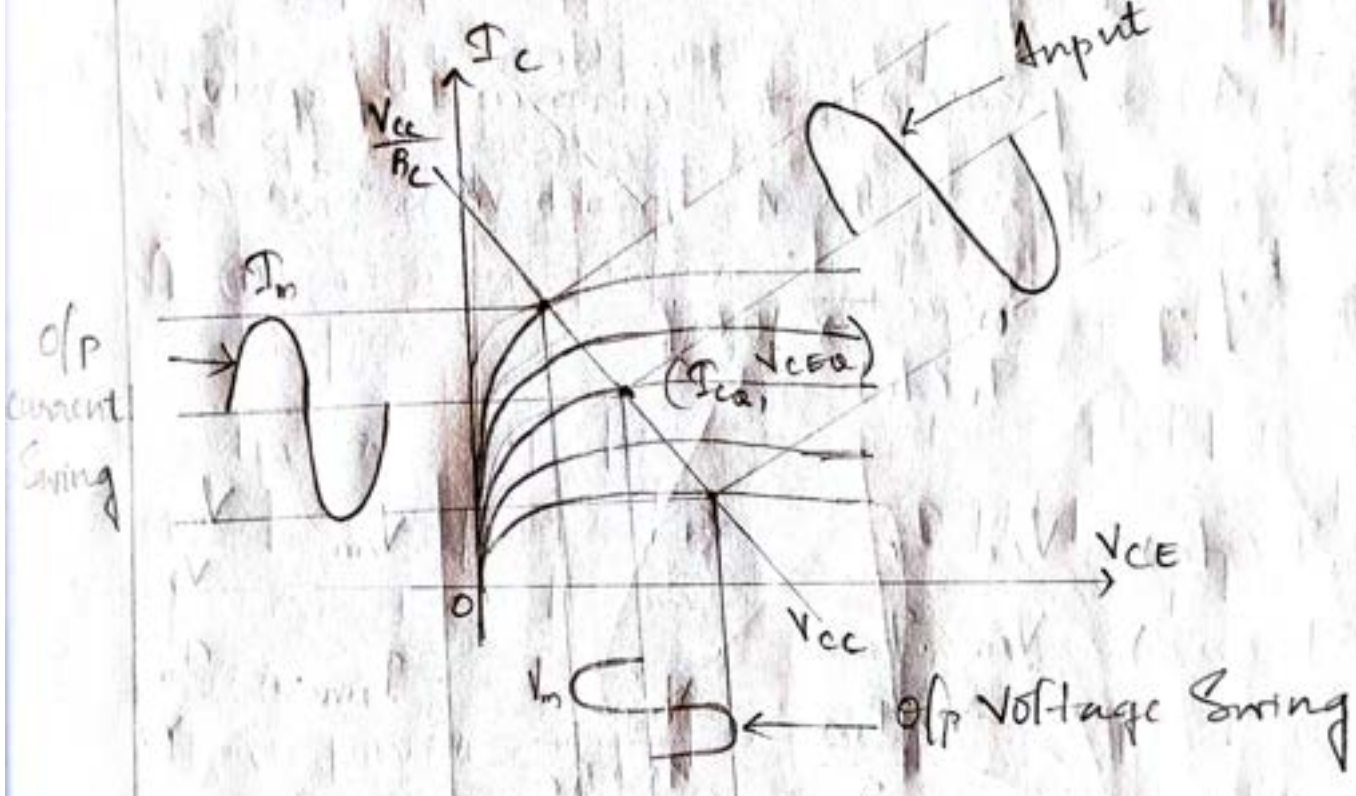


* Class D power amplifier.

Here the amplifier uses pulse signals which are ON for short interval and OFF for longer interval. The major advantage of class D operation is that the amplifier is ON (using power) only for short intervals and the overall efficiency can be very high.

Series fed Directly Coupled class A amplifer.





AC operation :

Here fixed biasing is used for the circuit and the resistance R_B is adjusted in such a way that the Q point lies exactly at the centre of load line. By applying KVL at i/p side

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B R_B - 0.7 = 0$$

$$I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \qquad I_{CQ} = \beta I_{BQ}$$

Applying KVL at the o/p side;

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE_Q} = V_{CC} - I_{CQ} R_C$$

Efficiency:

It represents the amount of power delivered or transfered to AC from DC source.

$$\% \eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100\%$$

$$P_{i(dc)} = V_{CC} \cdot I_C \quad \text{— (1)}$$

$$P_{o(ac)} = V_{rms} \cdot I_{rms}$$

$$= \frac{V_m I_m}{2} = \frac{V_{CC}^2}{4 \times 2 R_C}$$

$$P_{o(ac)} = \frac{V_{CC}^2}{8 R_C}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$V_m = V_{CC}/2$$

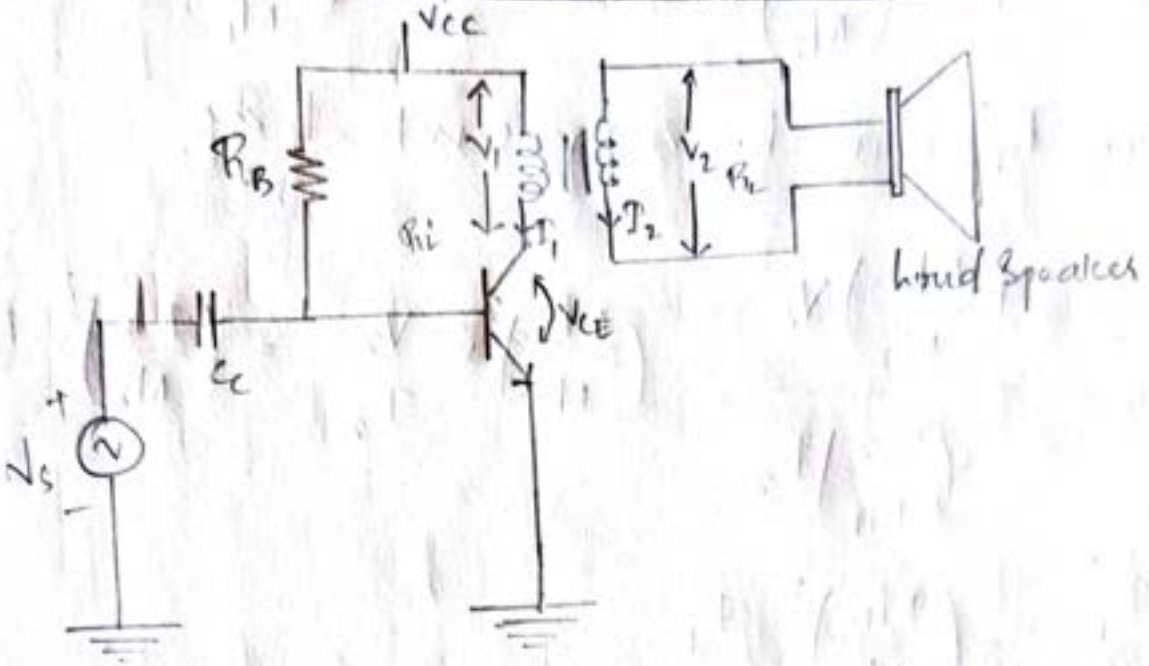
$$I_m = \frac{V_{CC}}{2R_C}$$

$$P_{i(dc)} = V_{CC} \times I_{CQ} = V_{CC} \times \frac{V_{CC}}{2R_C}$$

$$= \frac{V_{CC}^2}{2R_C},$$

$$\therefore \eta = \left(\frac{V_{CC}^2}{8R_C} \times \frac{2R_C}{V_{CC}^2} \right) \times 100 = 25\%$$

6/23 Transformer Coupled class A power amplifier.



Here instead of connecting load directly, connected through an o/p transformer. This transformer is used for impedence matching. The turns ration $\frac{N_1}{N_2}$ is so adjusted that the o/p impedence is perfectly matched with load impedence. Due to the transformer the load impedence R_L connected on the secondary reflected to the primary side as R_L' and act as it is actually connected in the primary side.

$$R_L = \frac{V_2}{I_2} \qquad R_L' = \frac{V_1}{I_1}$$

But from the transformer theory, we know

$$\boxed{\frac{V_1}{V_2} = \frac{N_1}{N_2} = \frac{I_2}{I_1}}$$

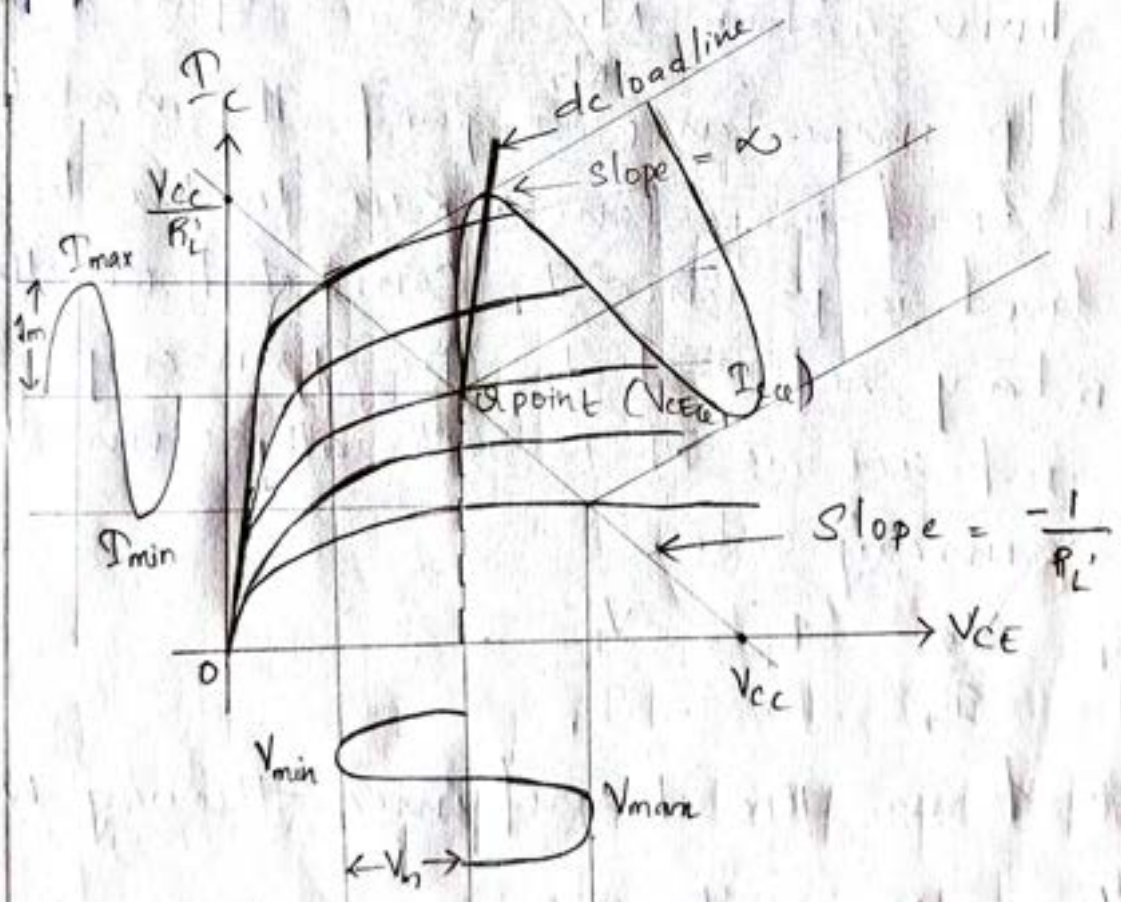
$$V_1 = \left(\frac{N_1}{N_2}\right) V_2 \qquad I_1 = \left(\frac{N_2}{N_1}\right) I_2$$

So R_L' can be represented as,

$$R_L' = \frac{\left(\frac{N_1}{N_2}\right) V_2}{\left(\frac{N_2}{N_1}\right) I_2} = \left(\frac{N_1}{N_2}\right)^2 \times \frac{V_2}{I_2} = \left(\frac{N_1}{N_2}\right)^2 \times R_L$$

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 \times R_L$$

i.e; by adjusting the turns ratio, we can make $R_L' = R_L$ and thereby can transfer maximum power to the load.



By applying KVL at the o/p side,

$$V_{CC} - I_{CQ} R'_{Ldc} - V_{CEQ} = 0$$

Since $R_{Ldc} = 0$, [at dc condition $R_L = 0$]

$$V_{CC} - V_{CEQ}$$

By applying KVL at the i/p side,

$$V_{CC} - I_{BQ} R_B - V_{BE} = 0$$

$$V_{BE} = 0.7$$

$$I_{BQ} = \frac{V_{CC} - 0.7}{R_B} \quad ; \quad I_{CQ} = \beta I_{BQ}$$

Efficiency

$$\eta = \frac{P_{o(ac)}}{P_{in(dc)}} \times 100\%$$

Input dc power =

$$P_{in(dc)} = V_{CC} \times I_{CQ} \quad \text{---(1)}$$

$$P_{o(ac)} = V_{rms} \cdot I_{rms}$$

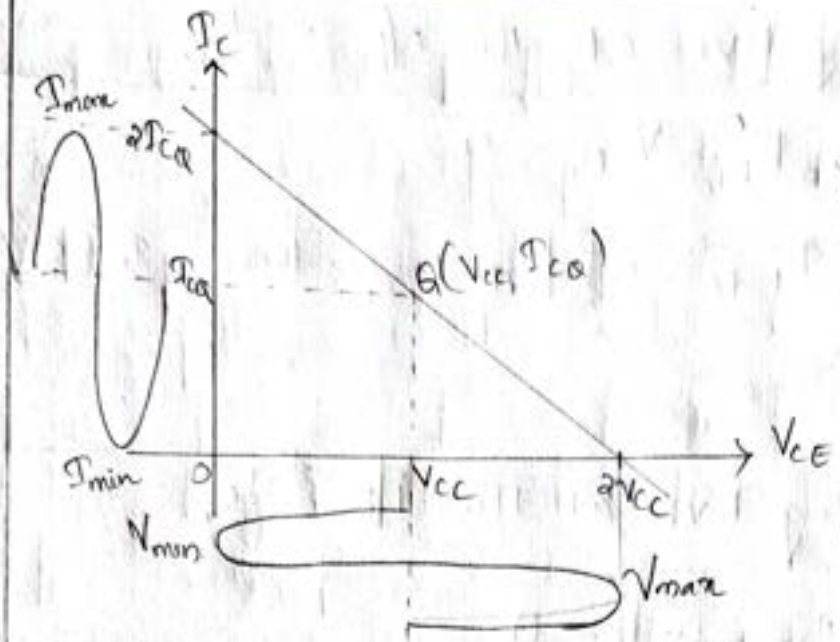
$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2}$$

$$= \frac{\left(\frac{V_{max} - V_{min}}{2}\right) \cdot \left(\frac{I_{max} - I_{min}}{2}\right)}{2} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8} \quad \text{---(2)}$$

$$\frac{(2)}{(1)} \quad \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 (V_{CC} \cdot I_{CQ})} \times 100\%$$

Maximum Efficiency.

$$\eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 (V_{CC} \cdot I_{CQ})} \times 100\%$$



$V_{max} = 2V_{cc}$

$V_{min} = 0$

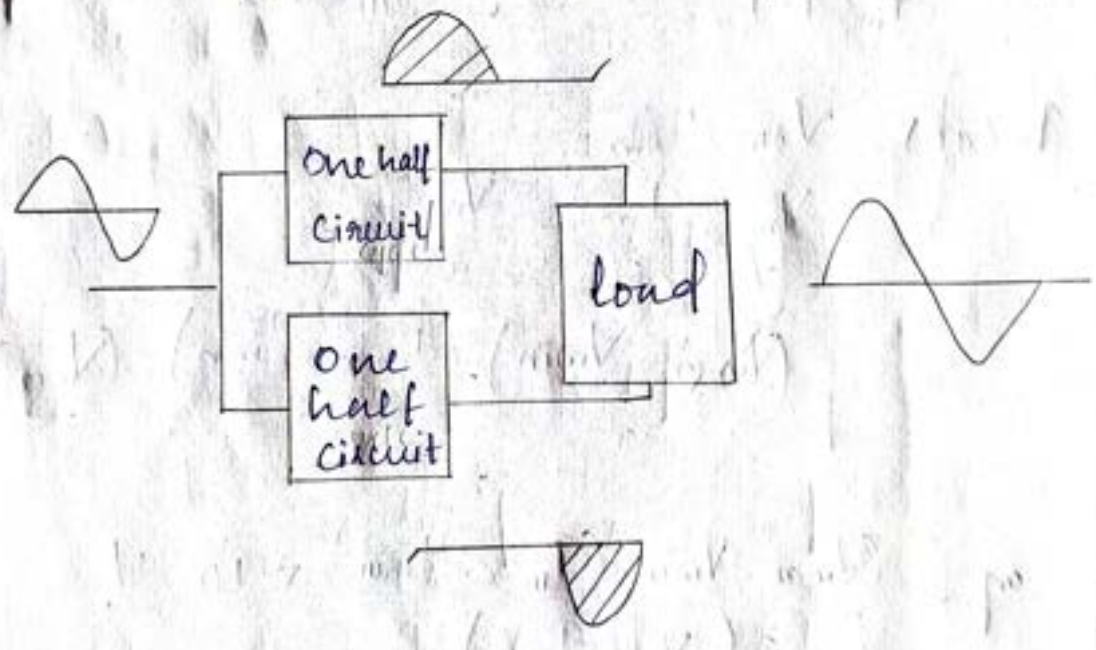
$I_{max} = 2I_{CQ}$

$I_{min} = 0$

$$\eta = \frac{2V_{cc} \cdot 2I_{CQ}}{8(V_{cc} \cdot I_{CQ})} \times 100 \quad (50)$$

$\eta = 50\%$

7/6/23 **Class B power amplifier:**

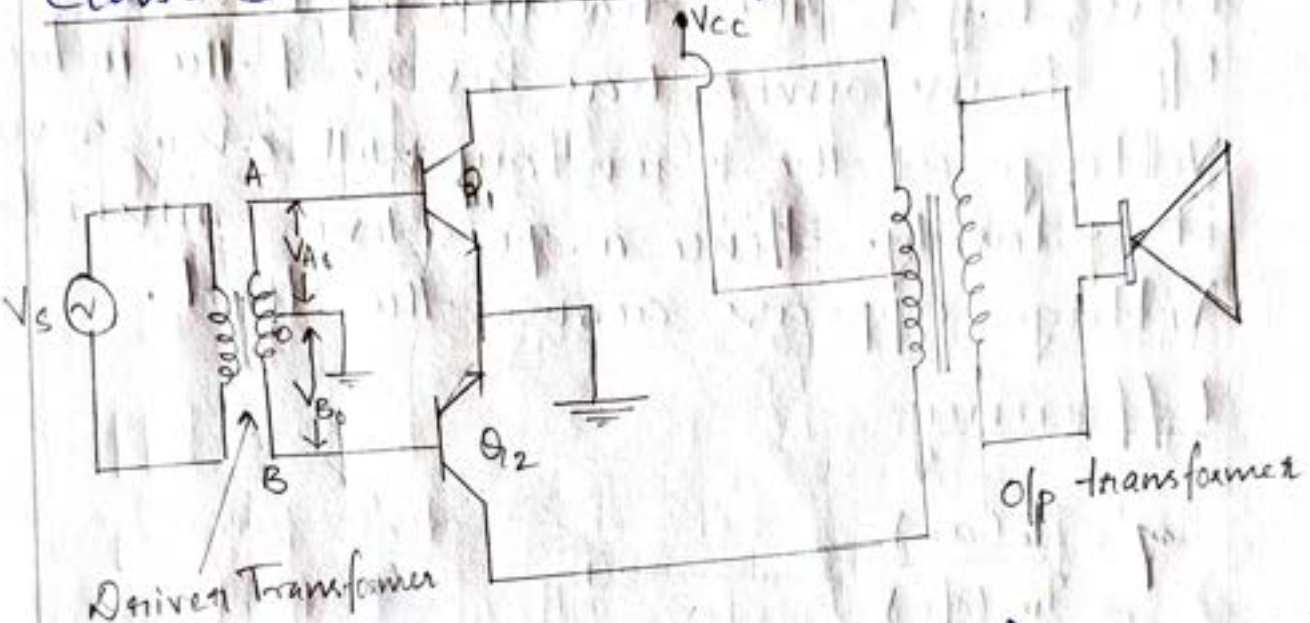


In class B operation transistor conducts current only for one half cycle of i/p signal. To obtain o/p it is necessary to use two transistors and have to operate on opposite half cycles. The combined operation provides

full cycle of o/p.

Since one part of the circuit push the signal high during one half cycle and the other half pull the signal to load. During the other half cycle, the circuit is refered as push-pull circuit

Class B Push-Pull amplifier.



Here two center tapped transformers were used in which the transformer in the i/p side is called driver transformer and the one at the o/p side is called output transformer.

Operation during +ve half cycle [$0 \le \omega t \le \pi$]

In the +ve half cycle of i/p the Secondary voltage of driver transformer V_{AO} is +ve and V_{BO} is -ve and so transistor Q_1 is forward biased and Q_2 is reverse biased. A Negative Sinusoidal voltage appears across the load.

Operation during -ve half cycle [$\pi \le \omega t < 2\pi$]

During -ve half cycle the polarity of induced voltage in Secondary winding of driver transformer gets reversed. Therefore Q_2 becomes forward biased and Q_1 becomes ~~re~~reverse biased. As the direction of current in the o/p transformer has reversed the induced voltage at the Secondary will also reverse its polarity. Hence a poisitive Sinusoidal voltage appears across the load.

Efficiency:

$$\eta = \frac{P_o(ac)}{P_{in}(dc)} \quad \text{——— (1)}$$

$P_{in}(dc) = V_{cc} \times$ Avg dc current ——— (2)

avg current $= \frac{1}{\pi}\int_0^{\pi} I_m \sin\omega t \, d\omega t$

$= \frac{I_m}{\pi}\left[-\cos\omega t\right]_0^{\pi}$

$= -\frac{I_m}{\pi}\left[\cos\pi - \cos 0\right]$

avg. current $= -\frac{I_m}{\pi}(-2) = \frac{2I_m}{\pi}$

Substitute in (2):

$P_{in}(dc) = V_{cc} \times \frac{2I_m}{\pi}$

$P_o(ac) = V_{rms} I_{rms} = \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$

$= \frac{V_m I_m}{2}$

$$\eta = \frac{V_m I_m/2}{V_{cc} \frac{2I_m}{\pi}} = \frac{V_m}{V_{cc}} \times \pi/4$$

For maximum efficiency the maximum o/p voltage swing $V_m = V_{cc}$

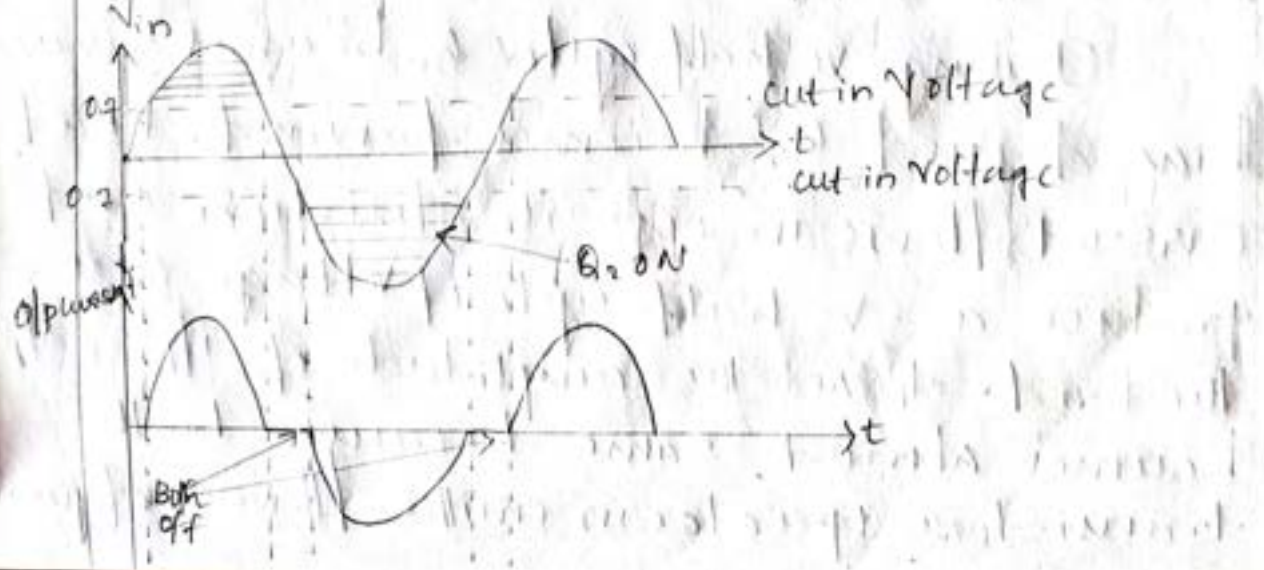
$$\therefore \eta = \frac{V_m}{V_m} \times \frac{\pi}{4}$$

$$\eta = 78.5\ \%$$

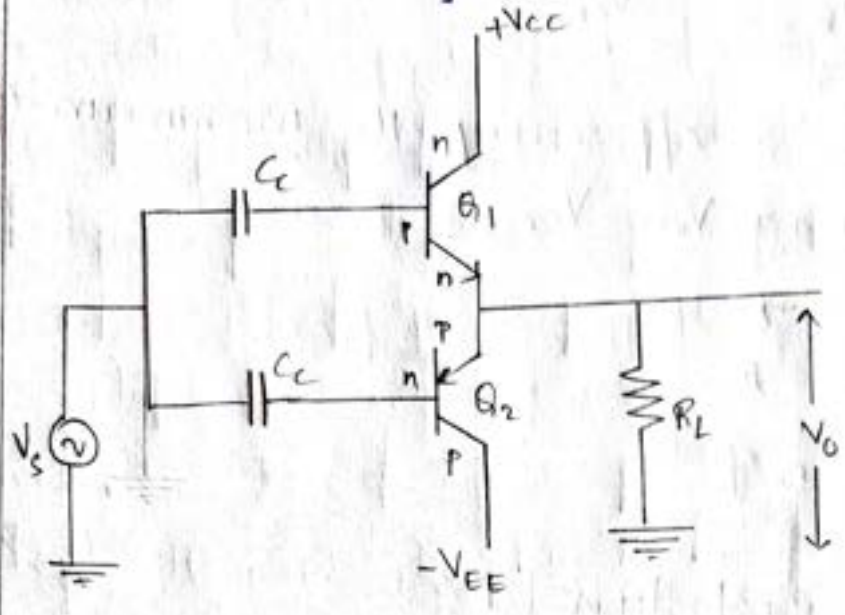
Cross over Distortion: [disadvantage of class B]

In class B power amplifier, the transistors are biased at cut off. To forward bias the transistor the i/p voltage must be greater than the cut in voltage of the junction [for Germanium - 0.2V and for Silicon - 0.7V]

As long as the i/p voltage is less than the cut in voltage, the transistors will remain in off state. Therefore, o/p gets distorted near zero crossings. This is known as cross over distortion.



Complementary Symmetry Class B.



This circuit uses a pnp and npp transistors. It doesnot use driver & o/p transformers and therefore also known as transformer less class push-pull amplifier. Here both transistors operates in emitter-follower configuration, for impedance matching.

During +ve half cycle Q_1 gets forward biased and Q_2 becomes reverse biased. Therefore, Q_1 conducts and produce +ve half cycle across the load.

During -ve half cycle Q_1 becomes reverse biased and Q_2 becomes forward. Load current flows in opposite direction and produce a -ve half cycle of voltage across the load. Here the amplitude of i/p & o/p becomes almost same because both transistors operates in emitter-follower configuration

Advantages:

* The impedance matching with load is possible as both transistors operates in emitter-follower configuration.
* Here transformers are not used which makes the circuit less expensive and less bulky.
* Even harmonics are automatically balanced hence only odd harmonics are present at o/p.

Disadvantages:

* Dual polarity supply is needed
* Q_1 and Q_2 should be matched in characteristics otherwise distortion will occur.
* Cross over distortion will be at the o/p.

Types of Distortion.

1. Amplitude Distortion or Non-linear Distortion.

Since the dynamic character of a transistor is non-linear, the o/p waveform of amplifier will be slightly different from AC i/p waveform. This type of distortion is known as Non-linear distortion or amplitude distortion.

Non-linear dynamic character of BJT

2. Frequency Distortion

The change in gain of amplifier with change in frequency of ~~Iput~~ input AC Signal is called frequency Distortion. Generally the low frequency and high frequency signals are alterated. The amplifier gain remains constant only in the mid range frequency. This distortion is caused by either internal initial capacitance of BJT or FET or Circuit capacitances.

3. Phase Shift Distortion

~~The change in gain~~ The phase shift introduced by amplifier for different I/p frequencies is not proportional to frequency. Thus phase distortion will takes place. Phase distortion are not detectable by human ears.

4. Harmonic Distortion.

The presence of frequency components (harmonics) in the O/p of an amplifier which are not present on its input side is known as Harmonic Distortion.

The frequency component which has the same frequency of input is known as fundamental frequency component (f_o). The other frequency components in the O/p which are multipliers of fundamental component ($2f_o, 3f_o, 4f_o, \ldots$) is the harmonics.

$2f_o$ - 2nd Harmonic

$3f_o$ - 3rd Harmonic

of waveform will be distorted with this presence of Harmonics. Amplitude of Harmonic component decreases with increase in the order of Harmonics.

Amplitude of fundemental component $= A_1$
Amplitude of Second Harmonic $= A_2$
Amplitude of third Harmonic $= A_3$
Amplitude of n^{th} Harmonic $= A_n$

then,

$$\% \text{ of } n^{th} \text{ Harmonic distortion } \% D_n = \frac{|A_n|}{|A_1|} \times 100$$

2^{nd} Harmonic distortion $\% D_2 = \frac{|A_2|}{|A_1|} \times 100$

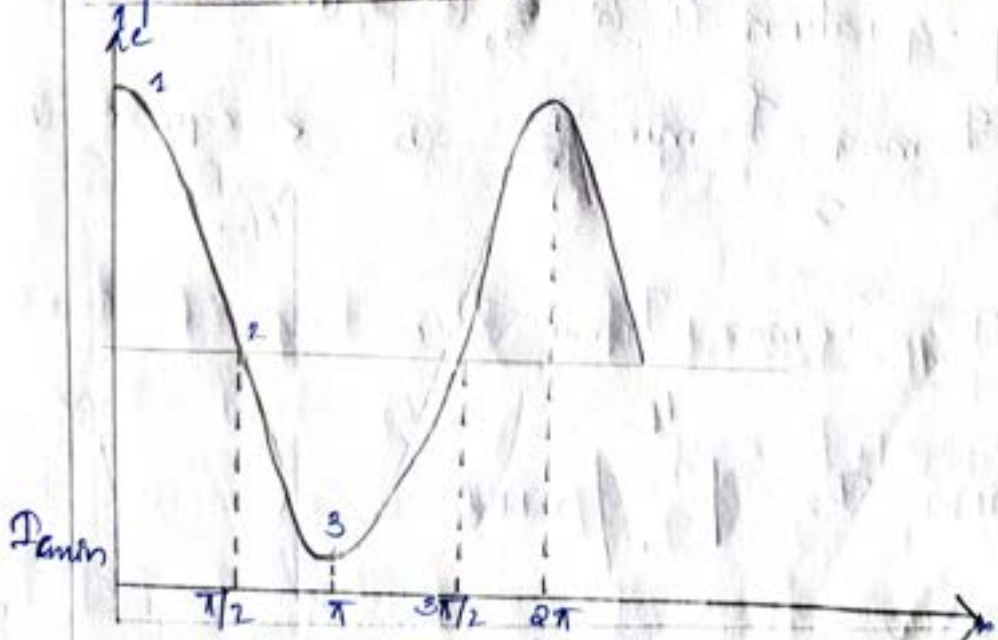
3^{rd} Harmonic distortion $\% D_3 = \frac{|A_3|}{|A_1|} \times 100$

Total Harmonic Distortion:

The effective value of distortion due to various harmonic components is given by total harmonic distortion :

$$\% \text{ THD} = \% D = \sqrt{D_2^2 + D_3^2 + \dots} \times 100$$

Expression for 2^{nd} Harmonic Distortion.



Waveform for obtaining 2nd Harmonic distortion

A collector current waveform with Quiscent, minimum & maximum and the time at which they occur is marked on the waveform.

Equation of distorted signal is

$$i_c = I_{CQ} + I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t \quad \text{——} (1)$$

at $\omega t = 0$

$$i_c = I_{c\max} = I_{CQ} + I_0 + I_1 \cos 0 + I_2 \cos 0$$

$$= I_{CQ} + I_0 + I_1 + I_2 \quad \text{——} (2)$$

at $\omega t = \pi/2$

$$i_c = I_{CQ} = I_{CQ} + I_0 + I_1 \cos \pi/2 + I_2 \cos 2\pi/2$$

$$I_{CQ} = I_{CQ} + I_0 - I_2 \quad \text{——} (3)$$

at $\omega t = \pi$

$$i_c = I_{c\min} = I_{CQ} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$

$$I_{c\min} = I_{CQ} + I_0 - I_1 + I_2 \quad \text{——} (4)$$

Solving equation (1), (2) & (3) & (4)

$$I_1 = \frac{I_{c\max} - I_{c\min}}{2} \quad \text{——} (5) \leftarrow \text{eqn } (2) - (4)$$

$$I_0 = I_2 - \frac{I_{c\max} + I_{c\min} - 2I_{CQ}}{4} \quad \text{——} (6) \leftarrow (2) + (3)$$

We know $D_2 = \left| \frac{I_2}{I_1} \right| \times 100$

$$D_2 = \left| \frac{\frac{1}{2}\left[I_{C max} + I_{C min}\right] - I_{CQ}}{I_{C max} - I_{C min}} \right| \times 100$$

In terms of collector voltages,

$$D_2 = \left| \frac{\frac{1}{2}\left[V_{CE max} + V_{CE min}\right] - V_{CEQ}}{V_{CE max} - V_{CE min}} \right| \times 100$$

6) Evaluate the Harmonic distortion components for an o/p signal having fundemental amplitude 2.5 V; 2nd Harmonic amplitude of 0.25 V, 3rd Harmonic amplitude of 0.1 V, 4th Harmonic of 0.5 V.

Sol:

$$\%D_2 = \frac{|A_2|}{|A_1|} \times 100 = \frac{0.25}{2.5} \times 100 = \underline{10\%}$$

$$\%D_3 = \frac{|A_3|}{|A_1|} \times 100 = \frac{0.1}{2.5} \times 100 = \underline{4\%}$$

$$\%D_4 V = \frac{|A_4|}{|A_1|} \times 100 = \frac{0.5}{2.5} \times 100 = \underline{20\%}$$

6) Calculate harmonic distortion for amplitude components $D_2 = 0.10$, $D_3 = 0.04$, $D_4 = 0.02$.

Sol:

$$\%\ THD = \sqrt{D_2^2 + D_3^2 + D_4^2 \ldots} \times 100$$

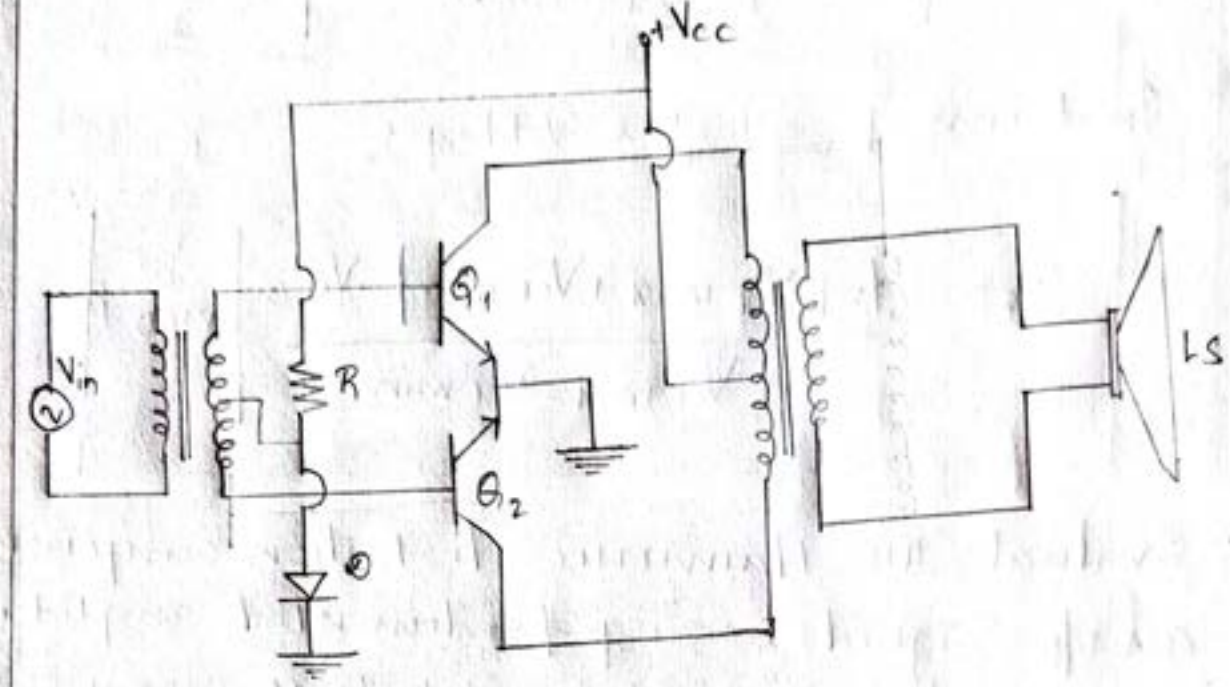
$$= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100$$

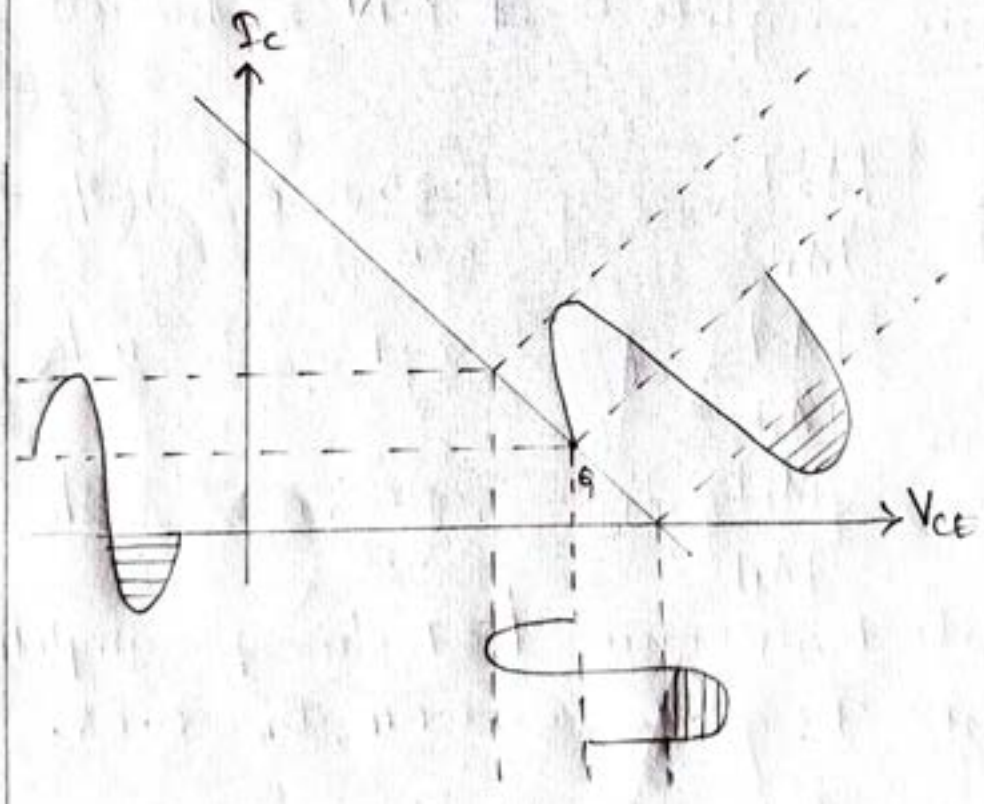
$$= 0.1095 \times 100$$

$$= 10.95\ \%$$

9/6/23

Class AB push-pull amplifier.

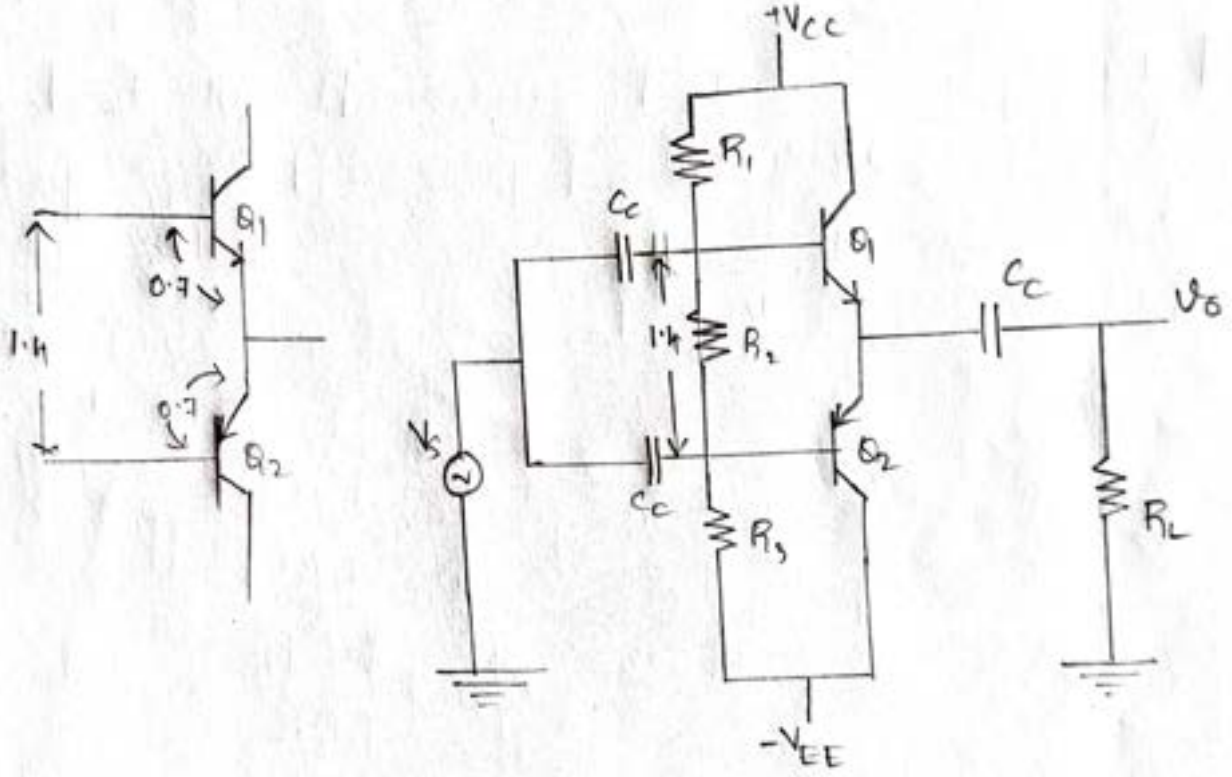




One of the main disadvantage of class B power amplifier is crossover distortion. In Class AB we use a diode to overcome the cross-over distortion of class B amplifier

The Dc voltage applied across diode D is connected to the base of two transistors through the secondary winding of driver transformer. This acts as bias for transistors and will conduct for complete half cycle of i/p to eliminate cross-over distortion. Due to this Q point is shifted slightly above x axis.

Complementary - Symmetry class AB



In order to make the base emitter junction of two transistors forward biased a voltage of 1.4 must appear across their bases. Here the value of R_1, R_2 and R_3 are so adjusted that a constant voltage of 1.4 appears across the resistor R_2 and there by enabling class AB operation.